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71	+VCCSA
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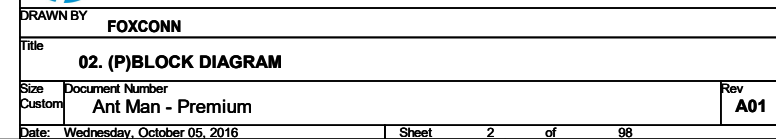
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PCB AND SILKSCREEN COLOR		
Program Phase	Color of PCB	Silkscreen
DB1	RED	YELLOW
DB2	RED	WHITE
DB3	RED	WHITE
SI1	GREEN	YELLOW
SI2	GREEN	WHITE
PI1	DARK BLUE	YELLOW
PI2+	DARK BLUE	WHITE
SPIMVB / PRODUCTION	DARK BLUE	WHITE

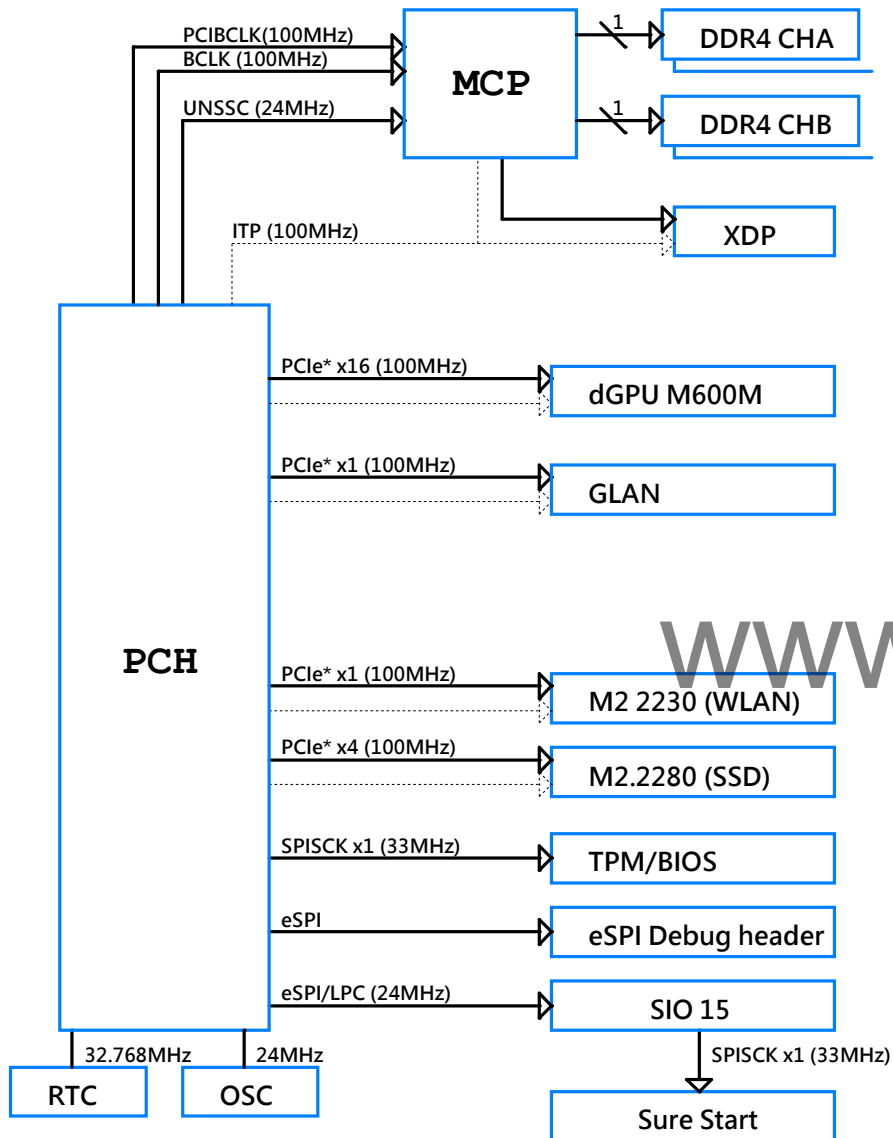
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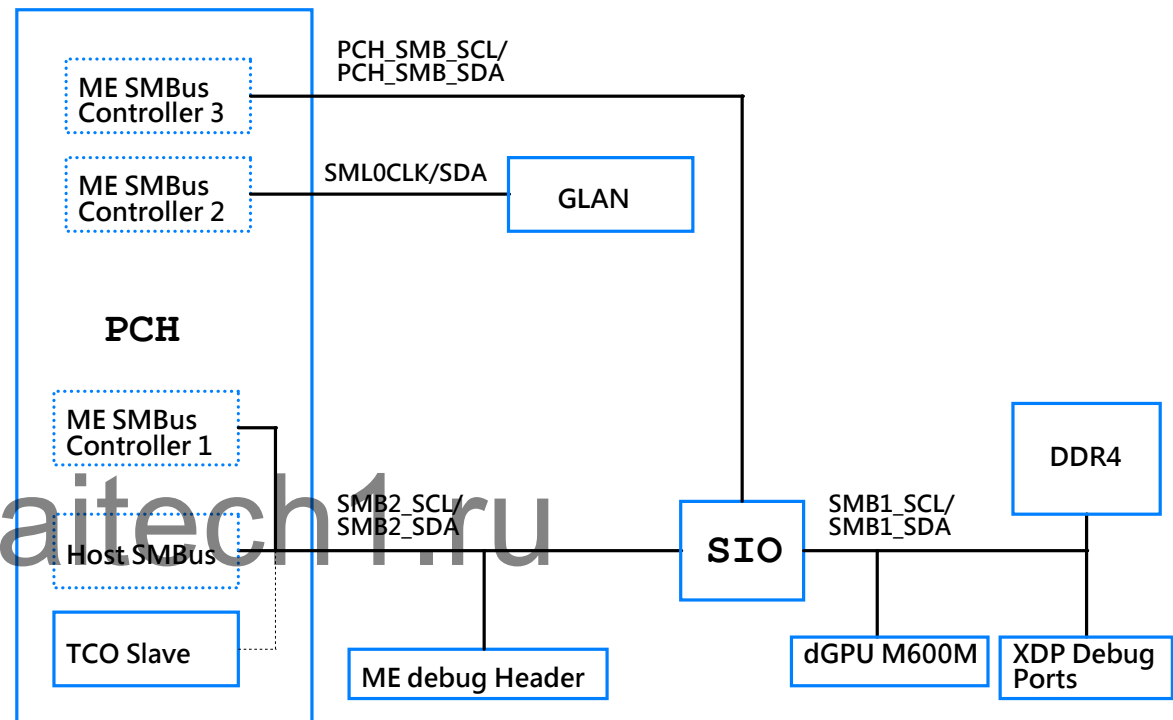
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Clock Diagram

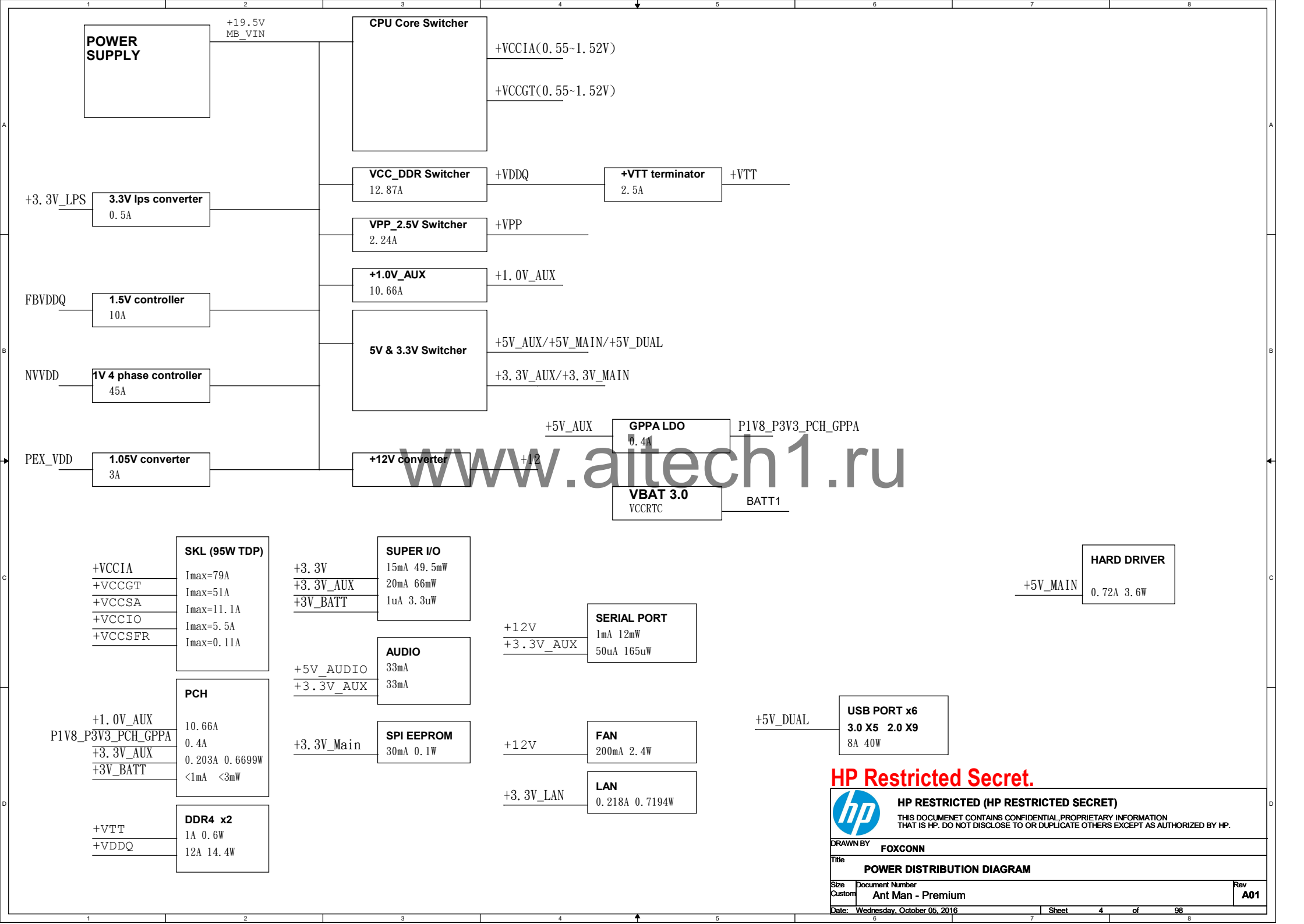


SMBus Block Diagram



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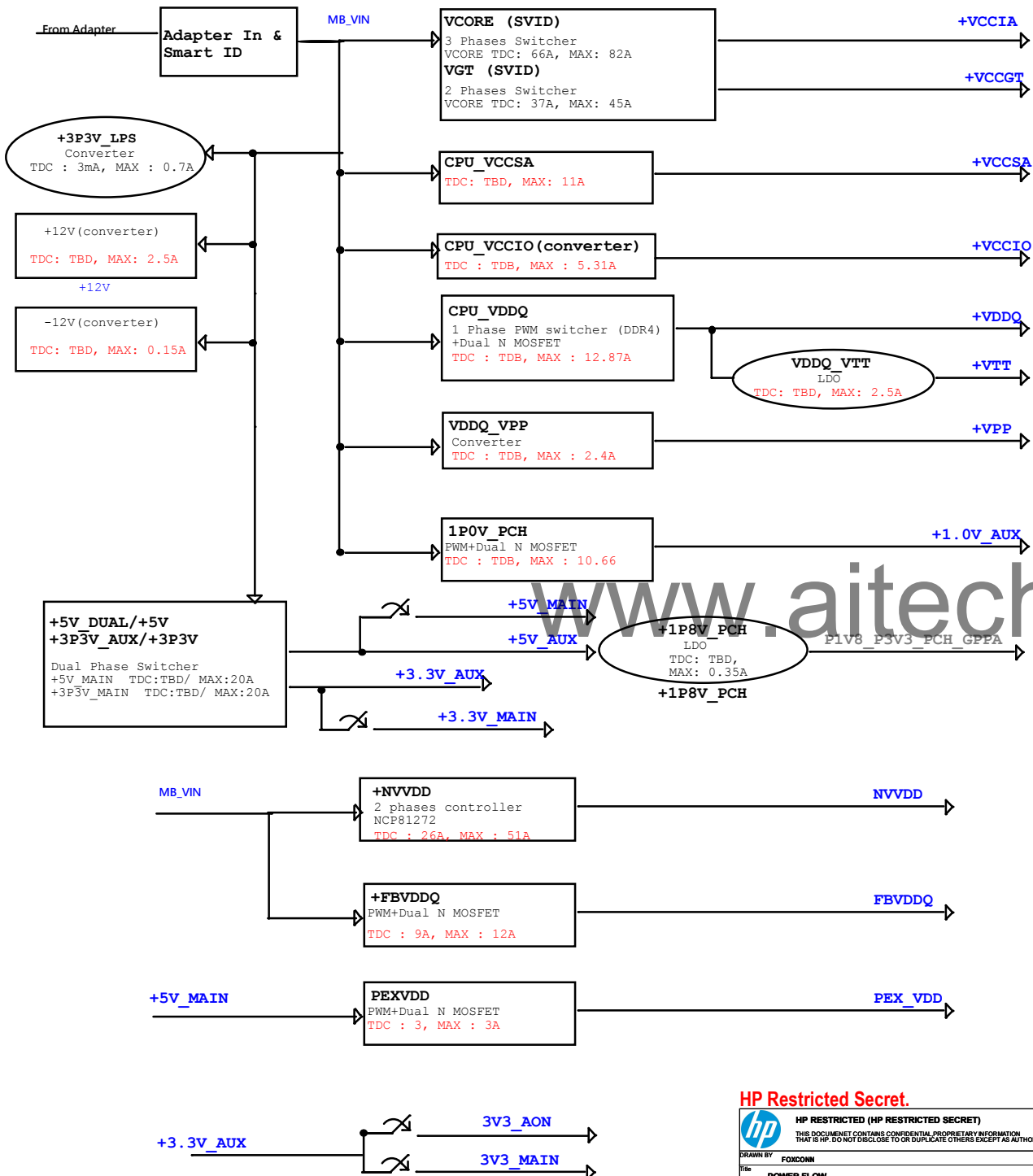
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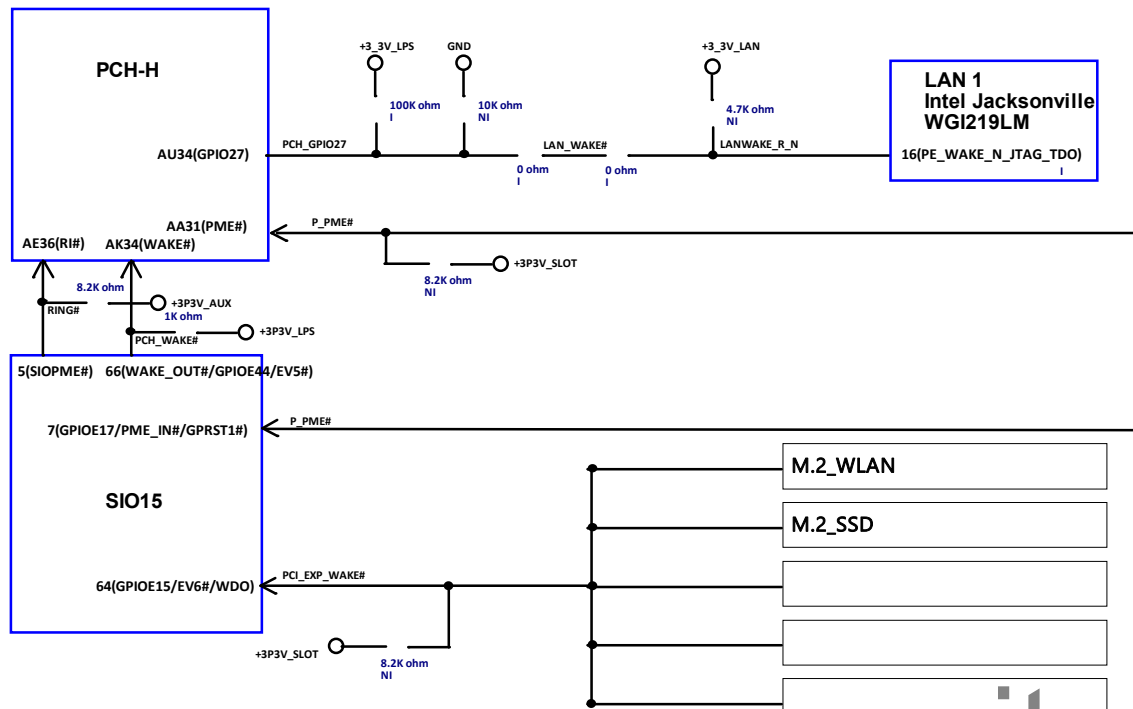
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Interrupt & PME diagram

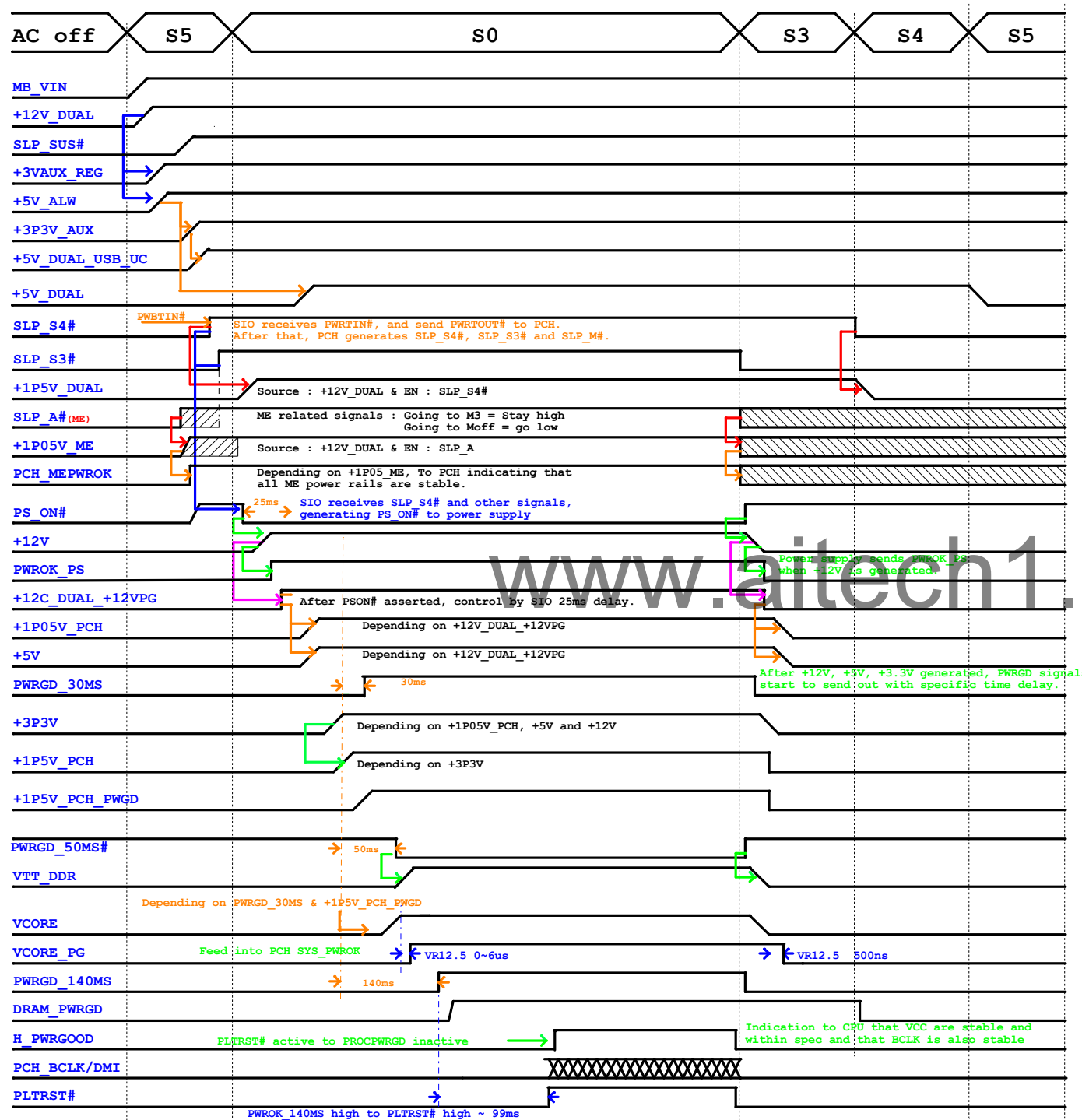


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POWER SEQUENCE DIAGRAM



POWER SEQUENCE DIAGRAM

1. MB_VIN ----> +5V_ALW
2. MB_VIN ----> +3P3V_LPS
3. PCH_DPWROK (SIO) ----> PCH
4. PWRBTN_IN# ----> SIO
5. PWRBTN_OUT# (SIO) ----> PCH
6. SLP_SUS# (PCH) ----> SIO
7. LPS_ON# (SIO) ----> +3.3V_AUX
8. LPS_ON# (SIO) ----> +5V_AUX
9. +5V_AUX ----> P1V8_P3V3_PCH_GPPA
10. +1P8V_AUX_PG ----> +1.0V_AUX
11. SIO_RSMRST# (SIO) ----> PCH
12. SUS_WARN# (PCH) ----> SIO
13. SUSACK# (SIO) ----> PCH
14. SLP_A# (PCH) ----> SIO
15. SLP_LAN# (PCH) ----> LAN
16. SLP_WLAN# (PCH) ----> WLAN
17. SLP_S5# (PCH) ----> SIO
18. SLP_S4# (PCH) ----> SIO
19. SLP_S4# (PCH) ----> +VDDQ
20. SLP_S4# (PCH) ----> +VPP
21. SLP_S4# (PCH) ----> +1P0V_VCCST
22. 5V_DUAL_EN (SIO) ----> +5V_DUAL
23. SLP_S3# (PCH) ----> SIO
24. SLP_S3# (PCH) ----> +VCCIO
25. SLP_S3# (PCH) ----> +VTT
26. VCCIO_PGOOD ----> +VCCSA
27. PS_ON# (SIO) ----> EN +12V_MAIN
28. +12V_PGOOD ----> EN +5V_MAIN
29. +5V_MAIN ----> +3.3V_MAIN
30. PWRGD_30MS ----> VCORE_EN
31. VCORE_EN ----> +VCCIA
32. VCORE_PG ----> VCCST_PWRGD_1V
33. VCORE_PG ----> PCH_PWROK
34. H_PWRGOOD (PCH) ----> CPU
35. PWRGD_170MS (SIO) ----> PCH
36. PLTRST_N (PCH) ----> SIO

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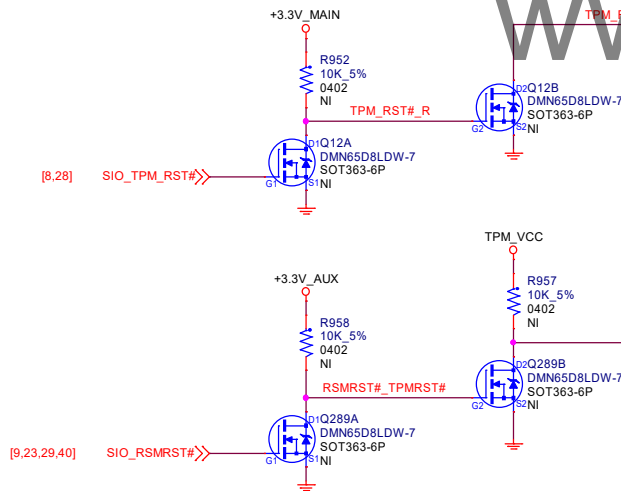
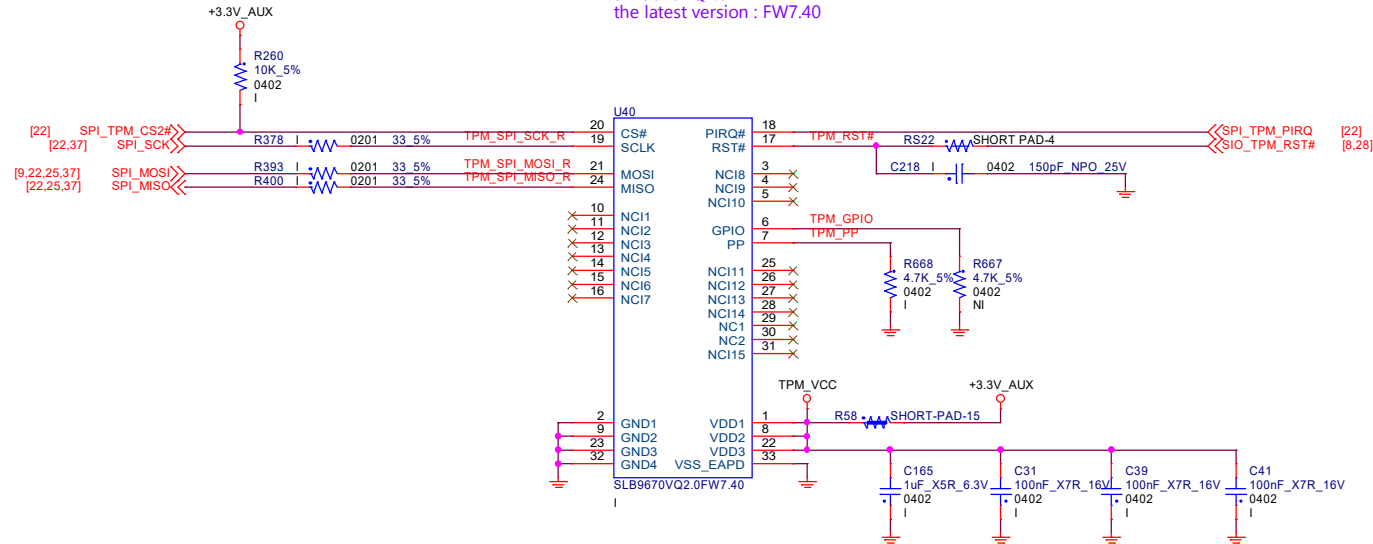
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TPM

SLB9670VQ2.0
the latest version : FW7.40



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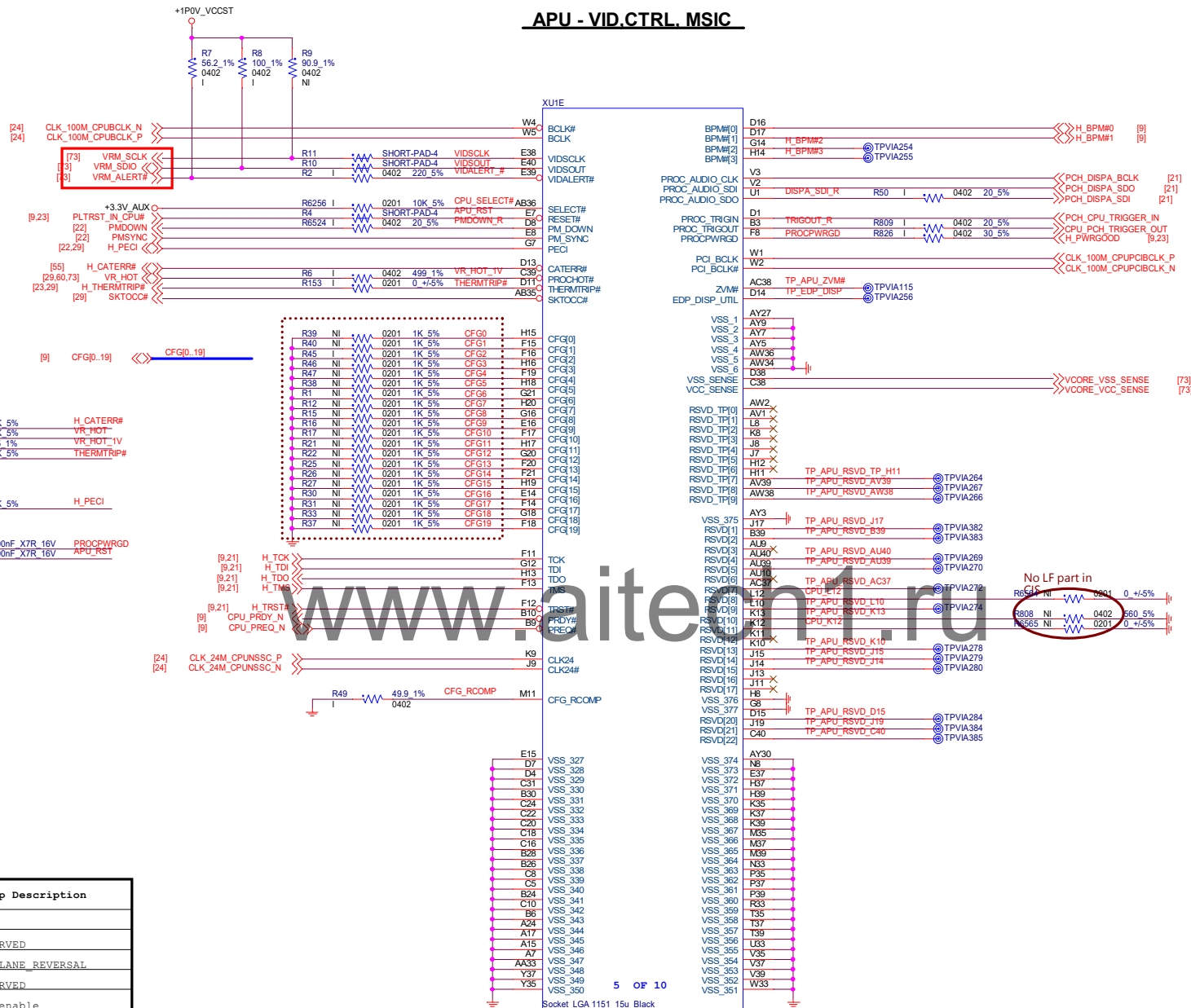
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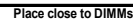
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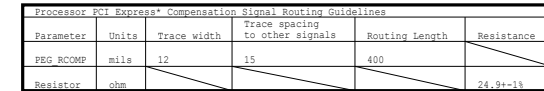
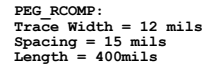
APU - VID.CTRL. MSC



DDR4 CH-B



PEG AC Cap Value	
Gen1/Gen2	75nf~265nf
Gen3	180nf~265nf

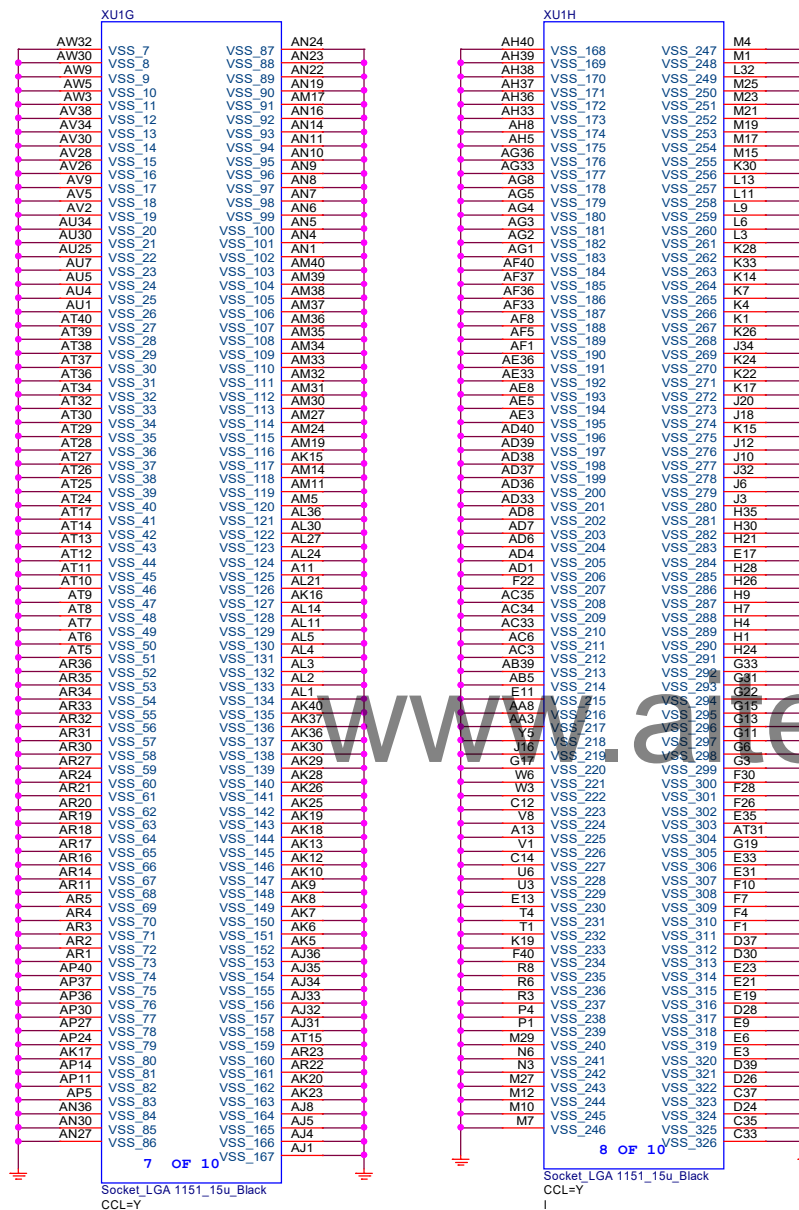


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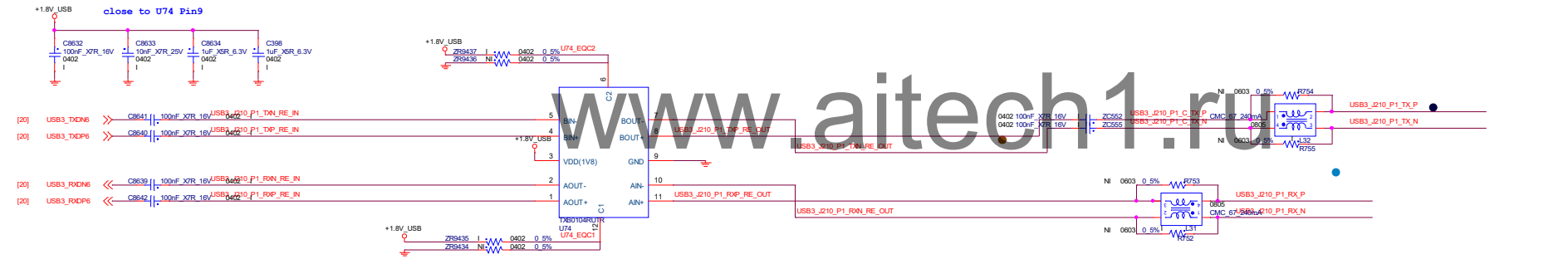
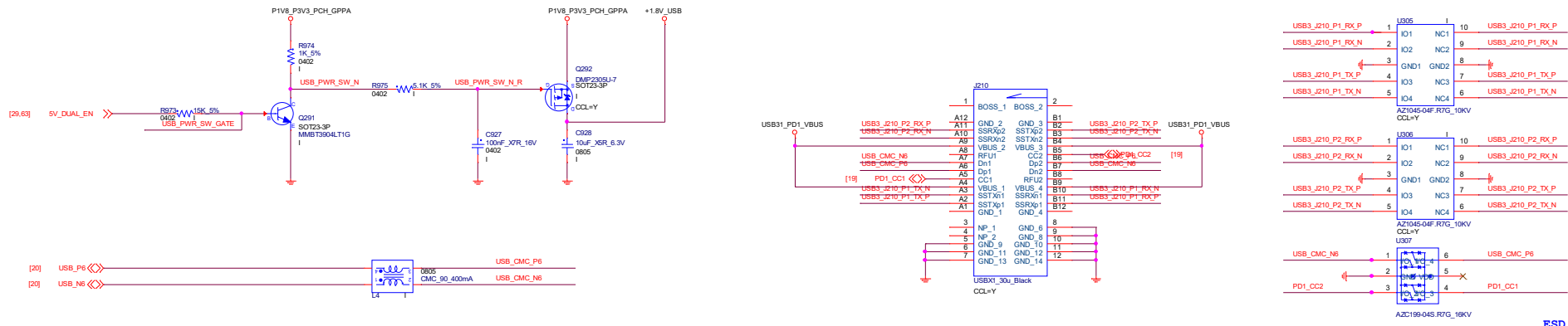
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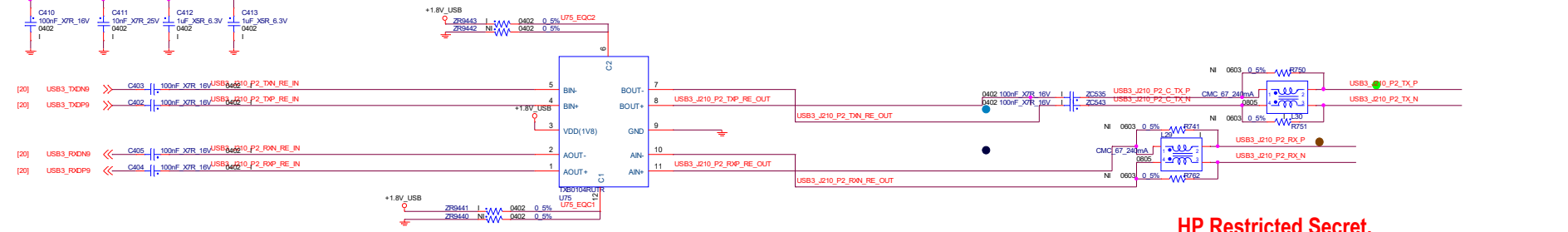


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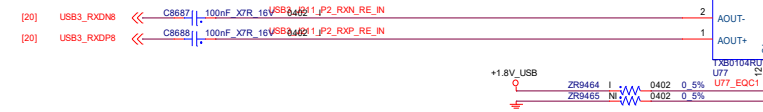
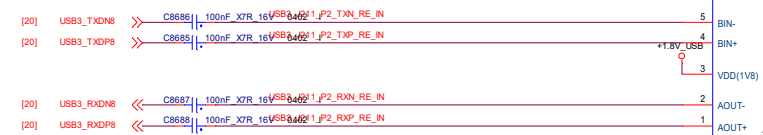
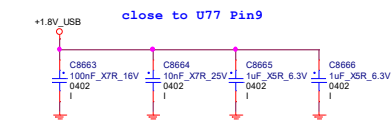
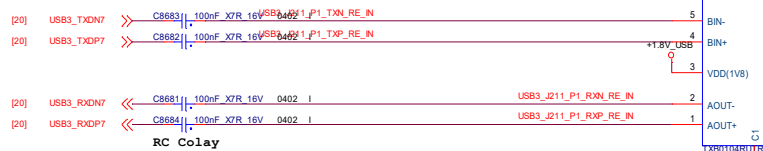
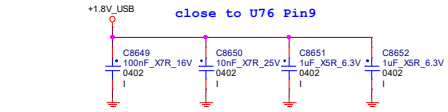
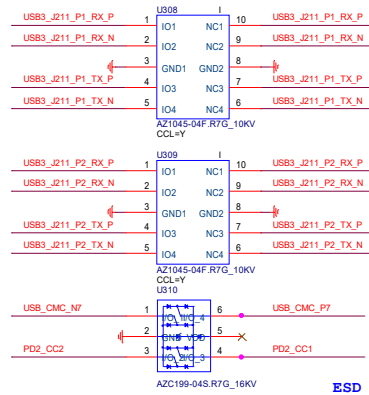
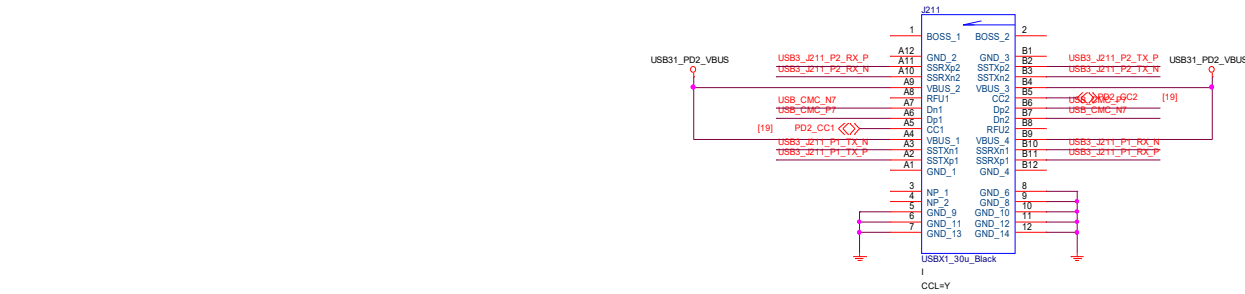
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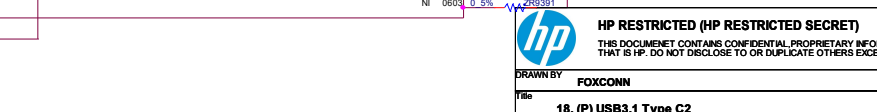
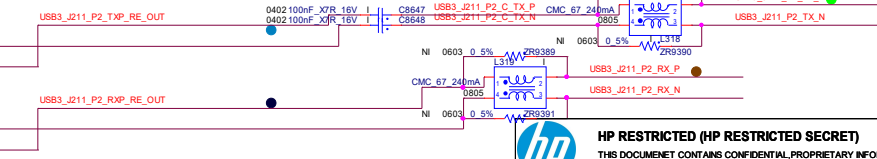
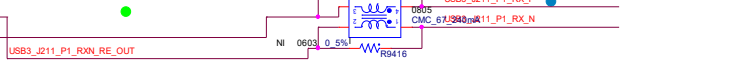
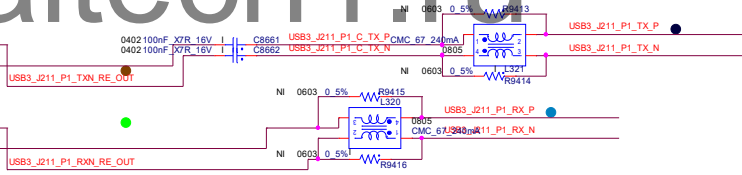
P26 USB 3.0 - Common Parts



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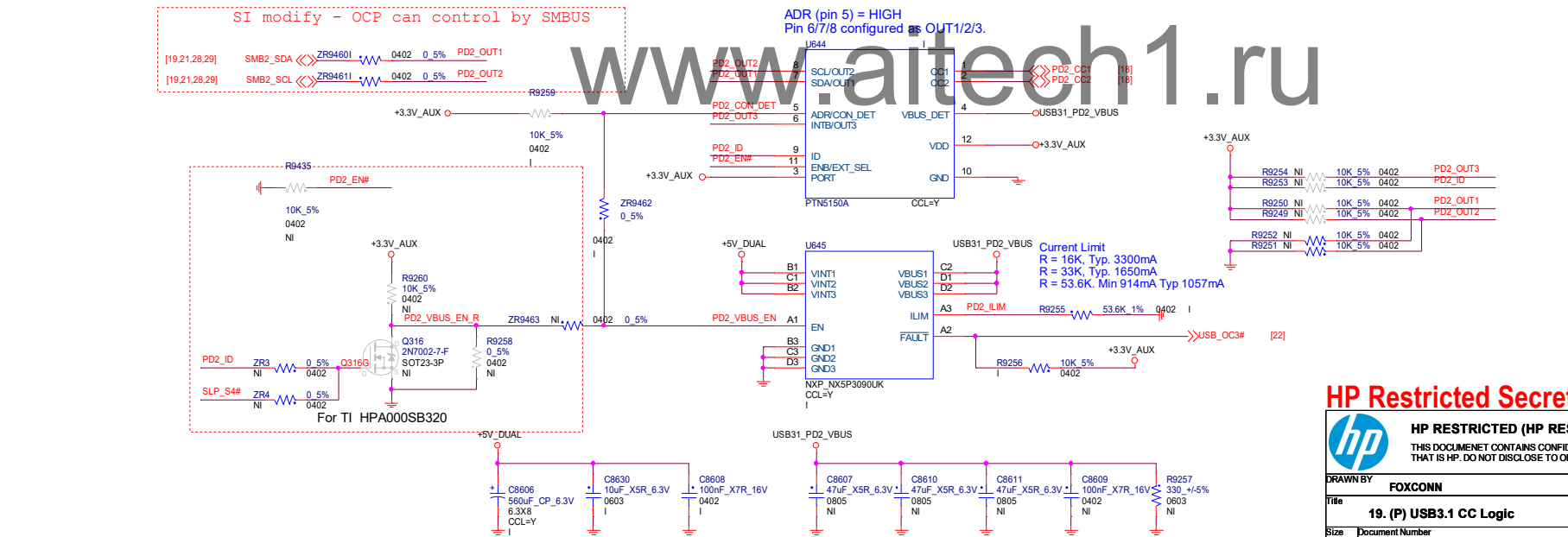
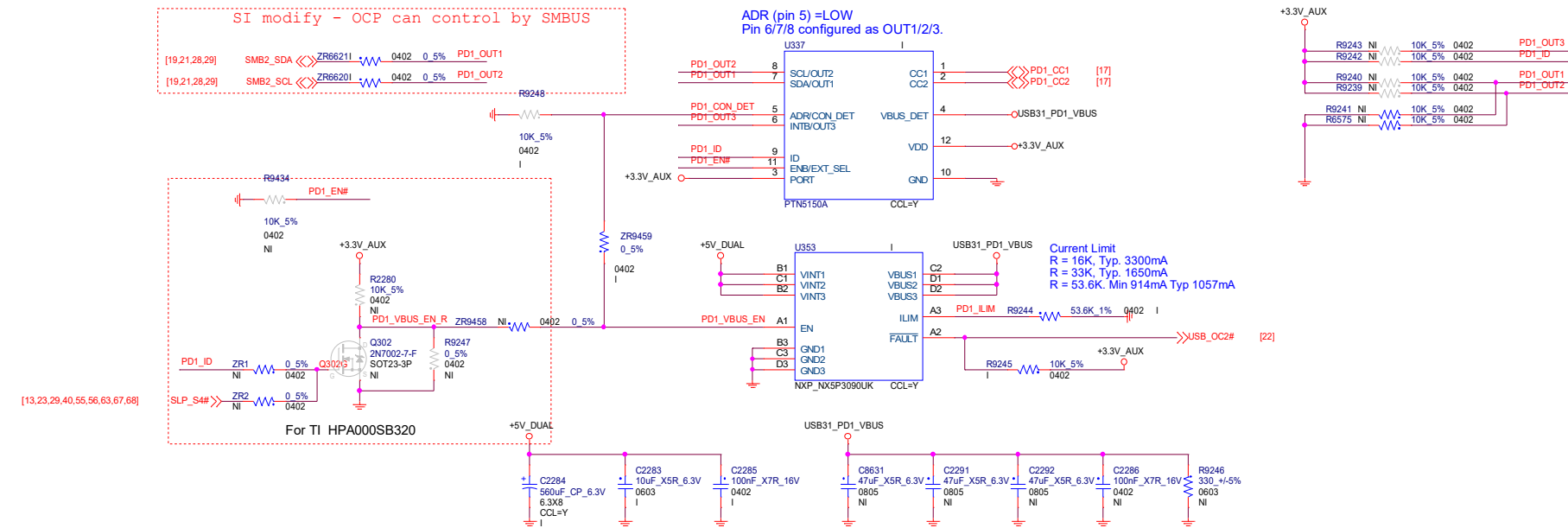
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USB TYPE-C CC LOGIC(PREMIUM ONLY)

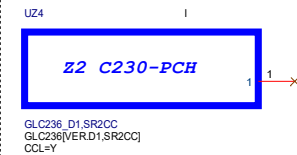
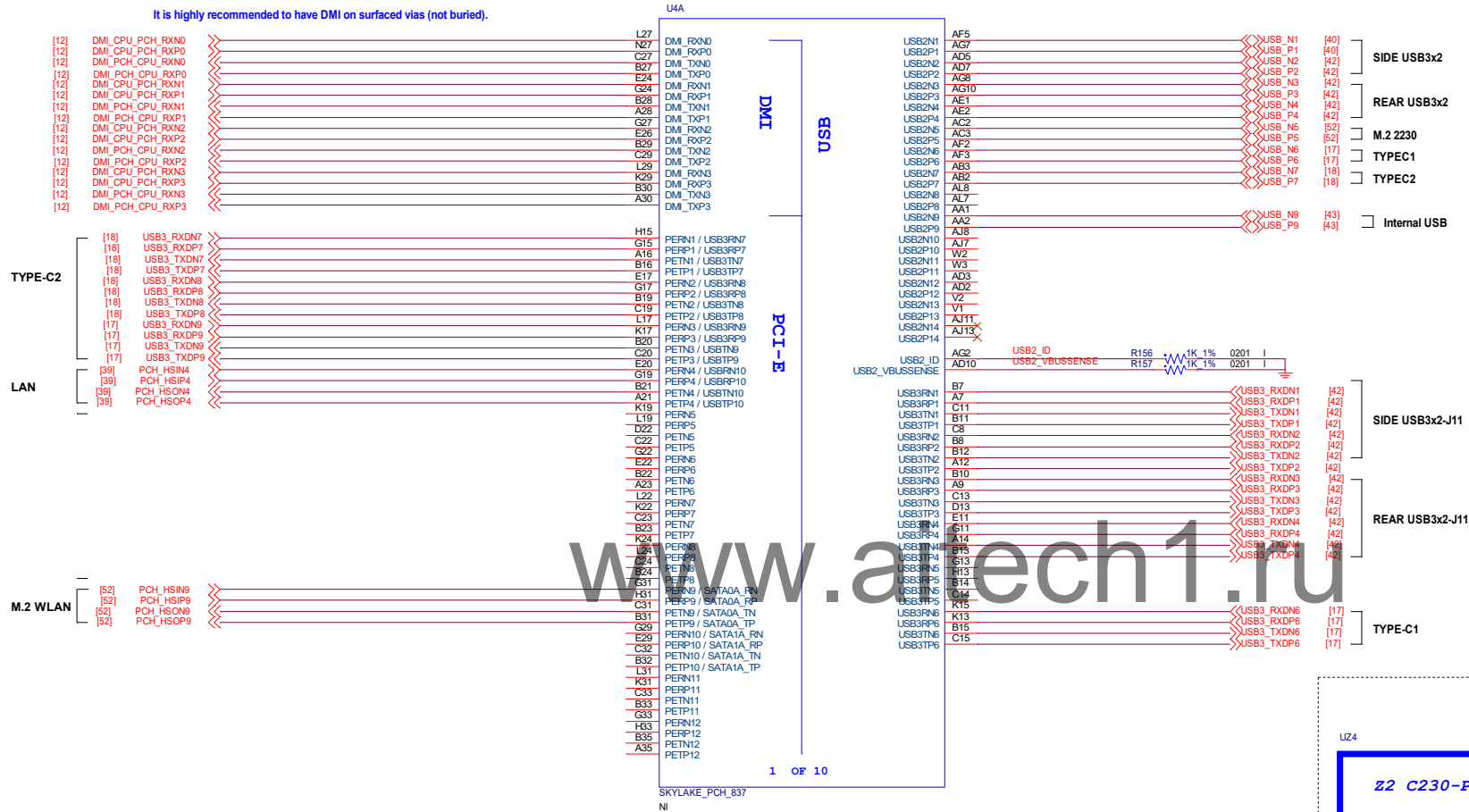


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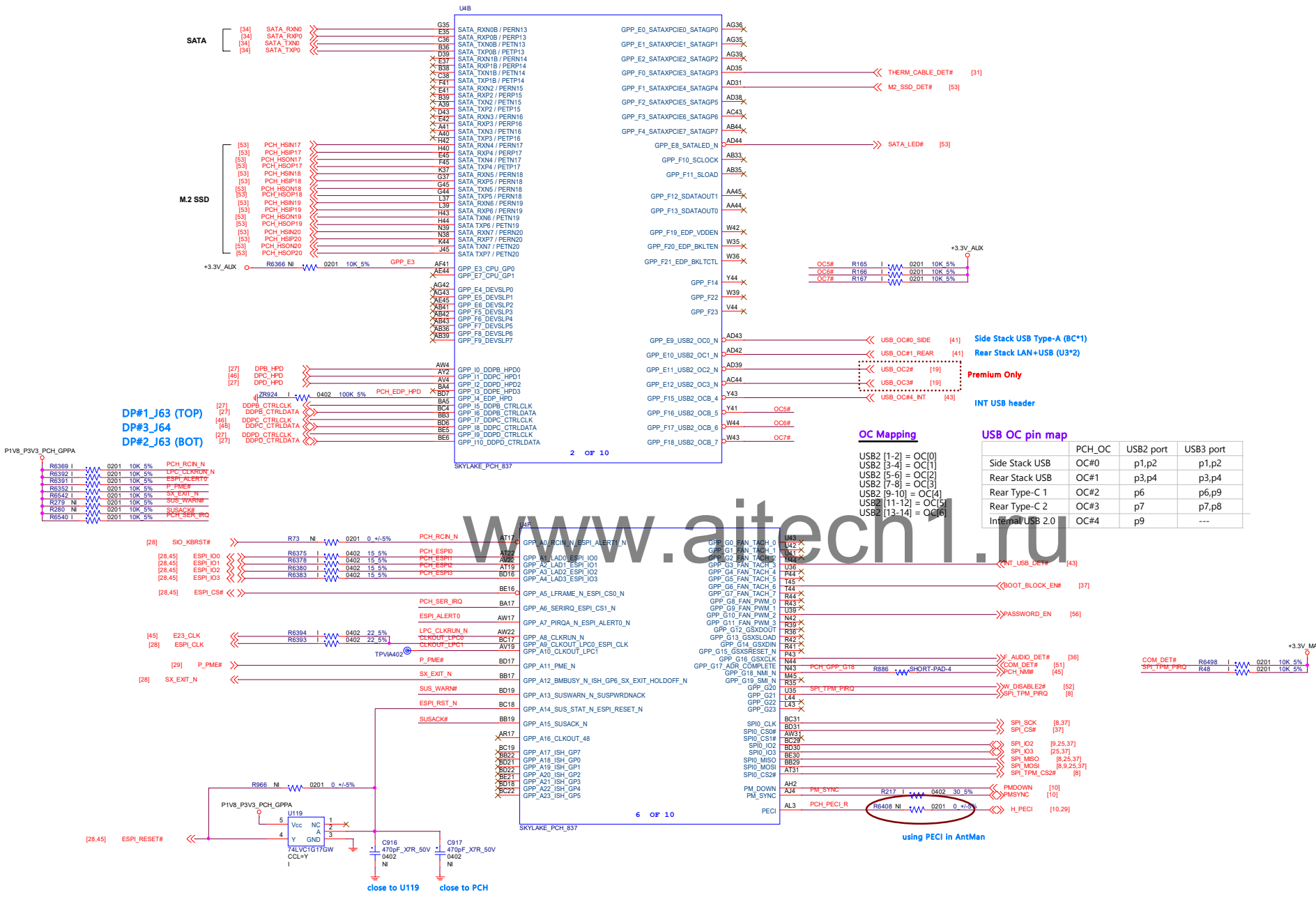
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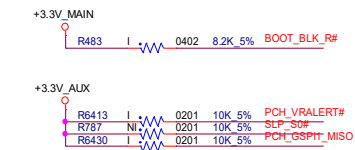
It is highly recommended to have DMI on surfaced vias (not buried).



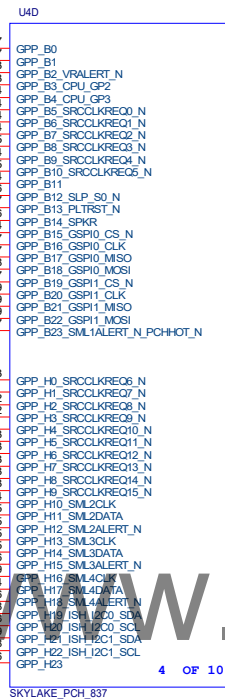
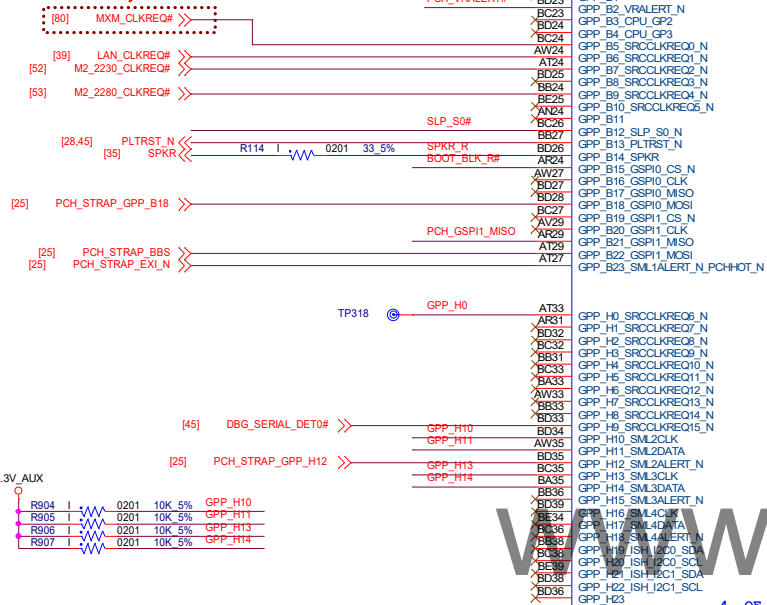
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Premium Only



U4C



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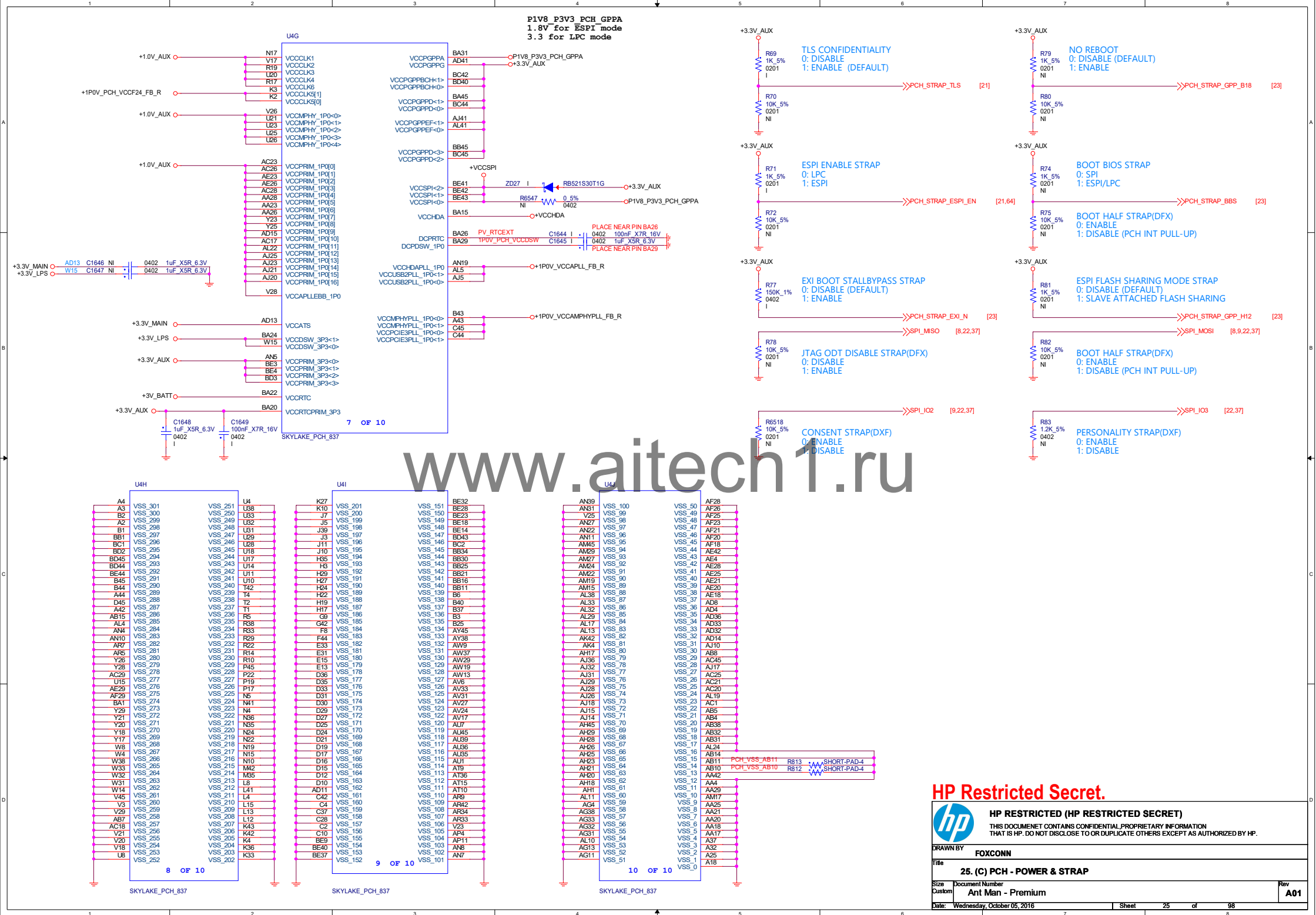
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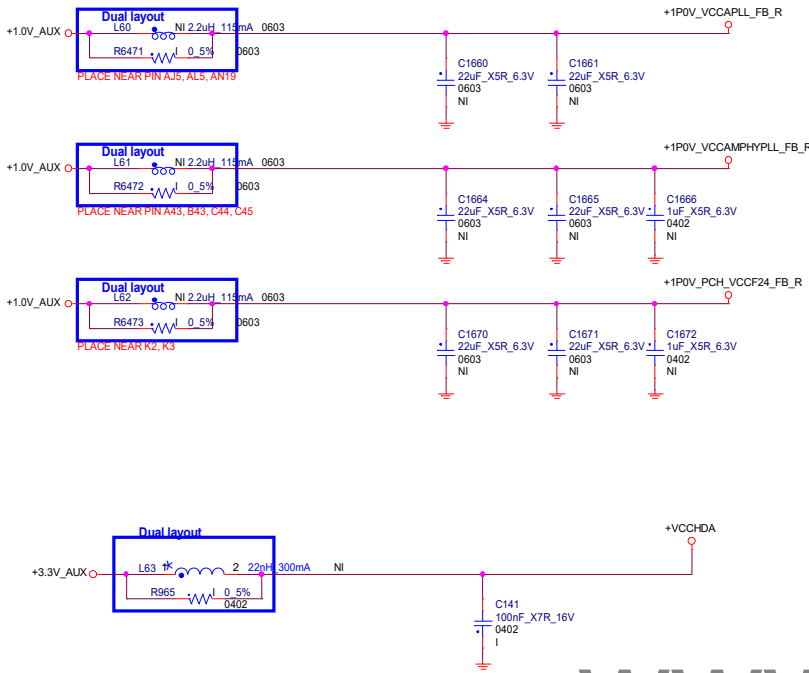
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SKYLAKE Decoupling & filter

FILTER

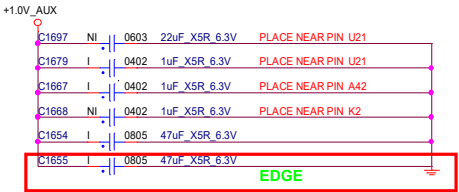


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Power Plane Isolation

Voltage	Interface	PCH Pins sharing power rail
VCC PCH 1.05V	Core	U26, U25, U23, U21, V26,
	PCIe/SATA/USB3	T19, T20, P22, P23, P25, P26, P28, P14, P16, P17
	GPIO/LPC	AC12
	FDI	M14
	DIFFCLK	U12, V14
		W14
		AB2
	SSC	T16, V16
PCH 3.3V Standby		AA16, W16
	USB2	AF19, AF20, AF22, AF23, AF22
	SUS	AM33, AN33
	USB2	AH18, AH20, AH22, AJ20, AK20
	AZALIA	AW26
PCH 3.3V	USB3	P20
	RTC	AP35
	CLK	AM7, AM9, AP5, AP7, AR4, AT5, AV4, AW4, AW9, AG12, AK11,
	HVMOS	AG1
	PCIe	AV3, AW3
	Core	U30, W30
	Fuse	AF26

V1.0A



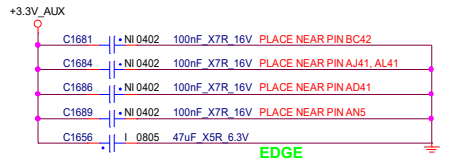
V3.3 DSW



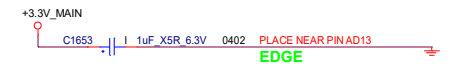
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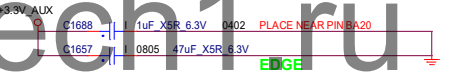
V1.8A / V3.3A



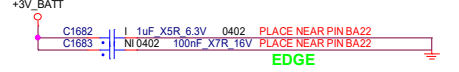
V1.8A / V1.8S / V3.3S



V3.3A



VCCRTC




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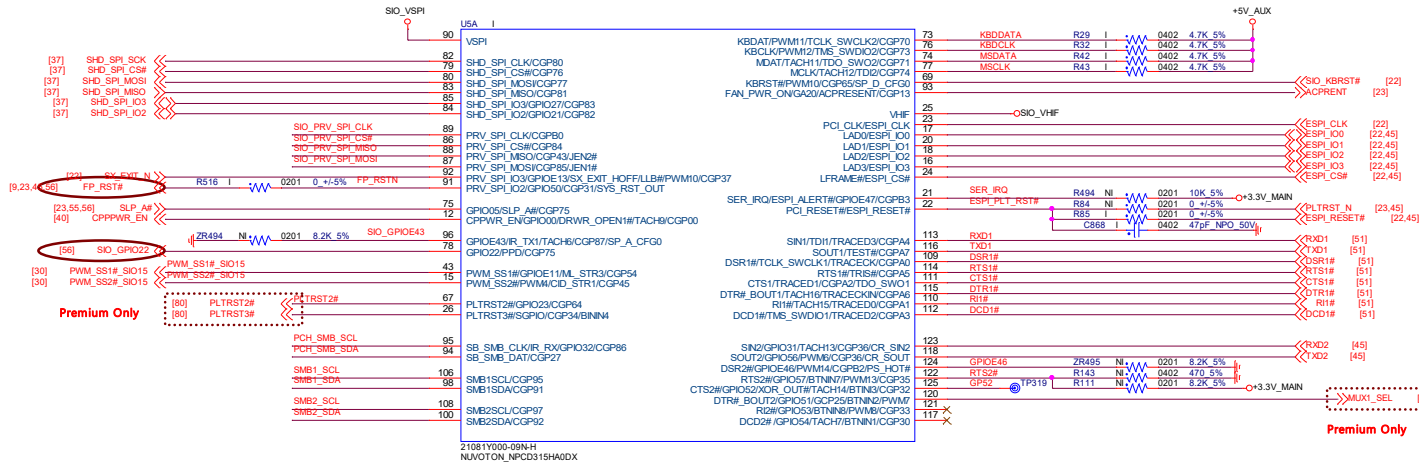


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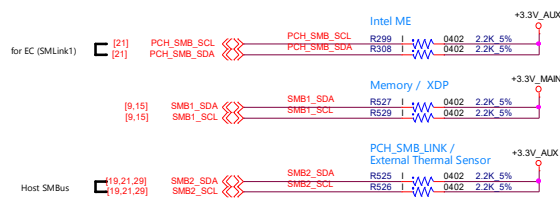
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SIO 15-A

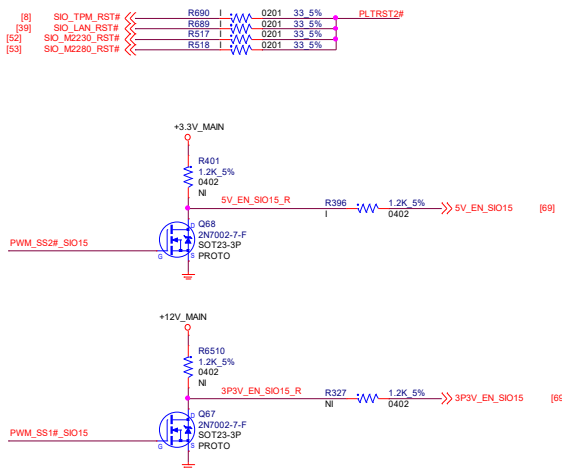


SIO Address
*2E/2F (Pull High)
*4E/4F (Pull-Low)

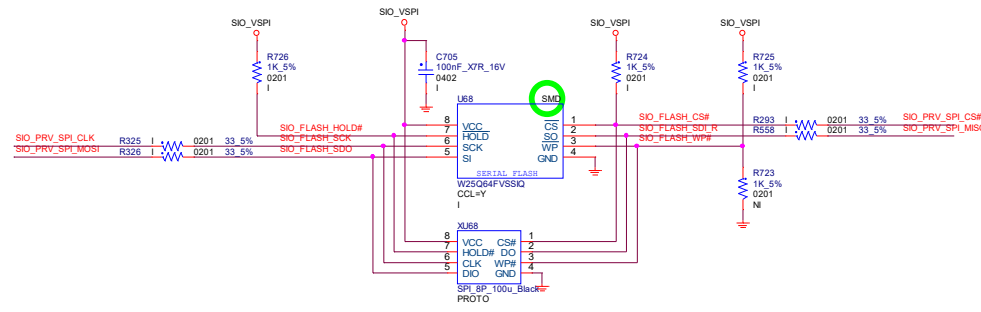
SM BUS PULL UP



PCIe Reset



SIO Flash ROM (Sure Start)



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28. (C) SIO15 (1)

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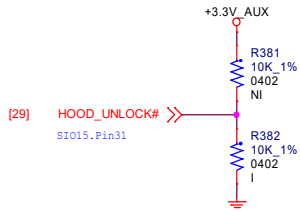
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Board ID

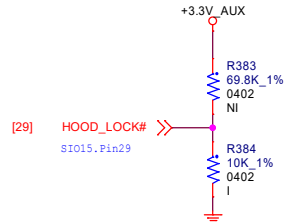
UNLOCK = ML_STR2
R108/R107 control PCA_ID_STS0[5:3]

LOCK = ML_STR1
R105/R106 control PCA_ID_STS0[2:0]

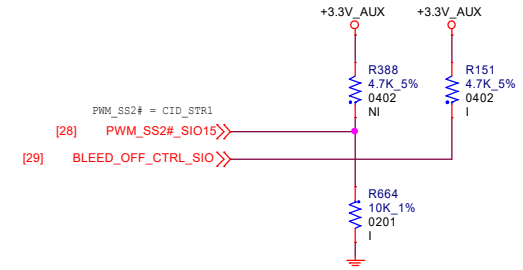
ML_STR2



ML_STR1



Chassis ID



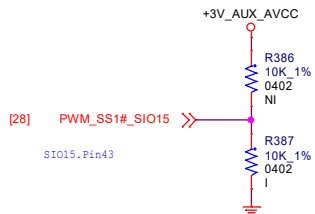
PCA_BRD ID Resistor values

Assignments	BRD_ID[1:0]	ML_STR2		ML_STR1	
		R381	R382	R383	R384
Premium	00	NI	10K	NI	10K
Reserved	01	NI	10K	69.8K	10K
Entry	10	NI	10K	30.1K	10K
Reserved	11	NI	10K	16.5K	10K

Rev ID

PWM_SS1# = ML_STR3
R436/R504 control PCA_REV_ID[2:0]

ML_STR3



PCA_REV_ID Resistor values

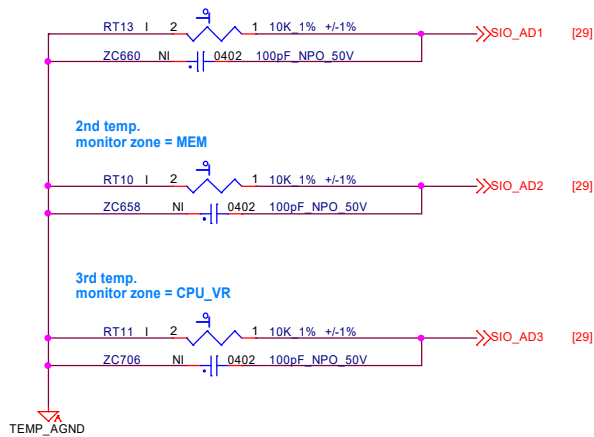
REV_ID	NPI	MP	ML_STR3		ML_STR3[2:0]b Register Value
			PU 1%	PD 1%	
0	DB-1	MVB, A	NI	10K	000
1	DB-2	1stECN	69.8K	10K	001
2	DB-3	2ndECN	30.1K	10K	010
3	SI-1	3rdECN	16.5K	10K	011
4	SI-e	4thECN	16.5K	16.5K	100
5	SI-3	5thECN	10K	16.5K	101
6	PV-1	6thECN	10K	30.1K	110
7	PV-2	7thECN	10K	69.8K	111

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Size	Document Number	Rev	
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THERMAL SENSORS (SIO15)

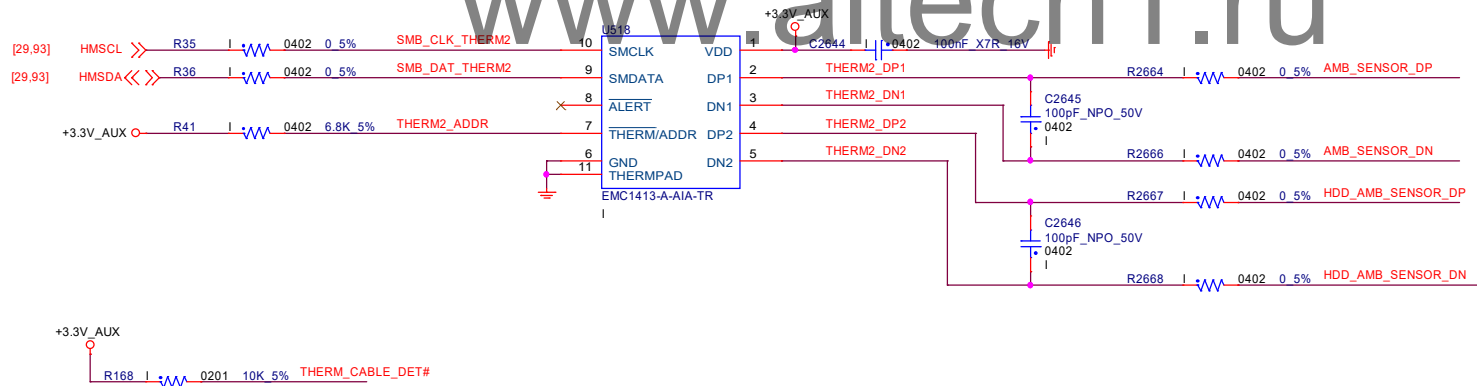
1st temp.
monitor zone = M2_SSD



2nd temp.
monitor zone = MEM

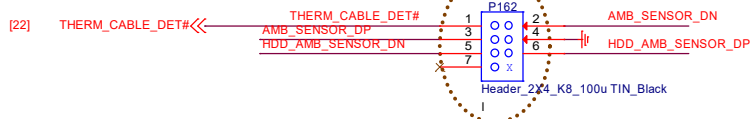
3rd temp.
monitor zone = CPU_VR

4th temp.
monitor zone = GPU



Via Cable, 5th temp.
monitor zone = System Ambient

Via Cable, 6th temp.
monitor zone = HDD Ambient




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Title		31. (C) SIO15 (4)	
Size	Document Number	Rev	
Custom	Ant Man - Premium	A01	
Date:	Wednesday, October 05, 2016	Sheet	31 of 98

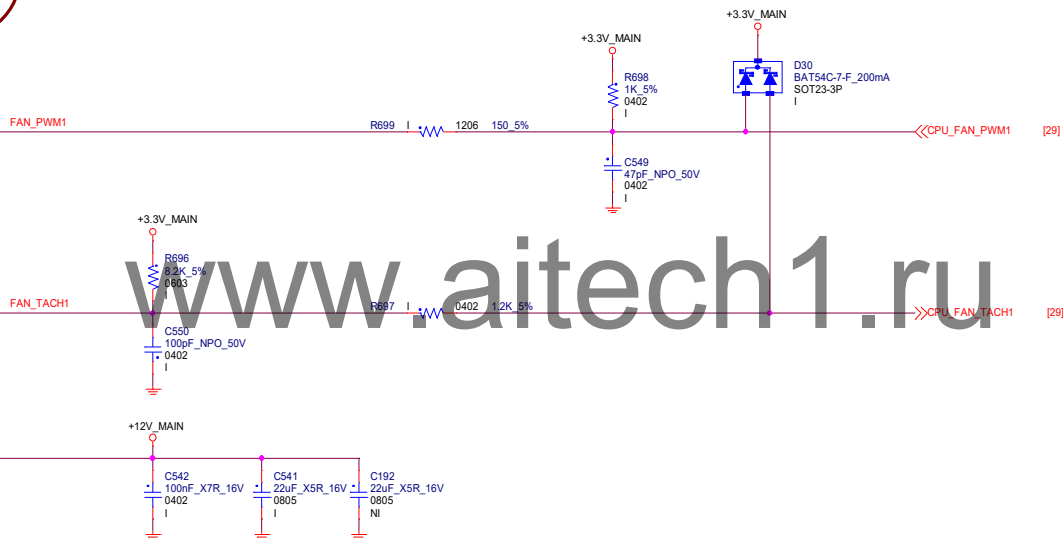
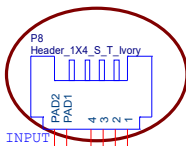
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CPU Fan

1	FAN PWM INPUT
2	FAN TACH
3	+12V
4	GND

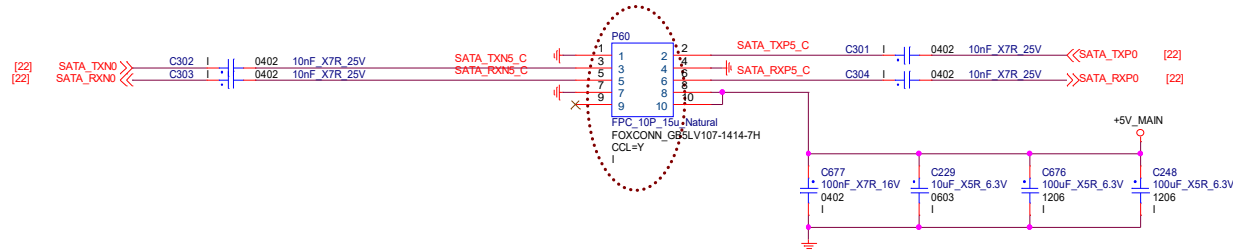


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Title 33. (C) FAN	
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Combo SATA Header


Rear HDD LED header



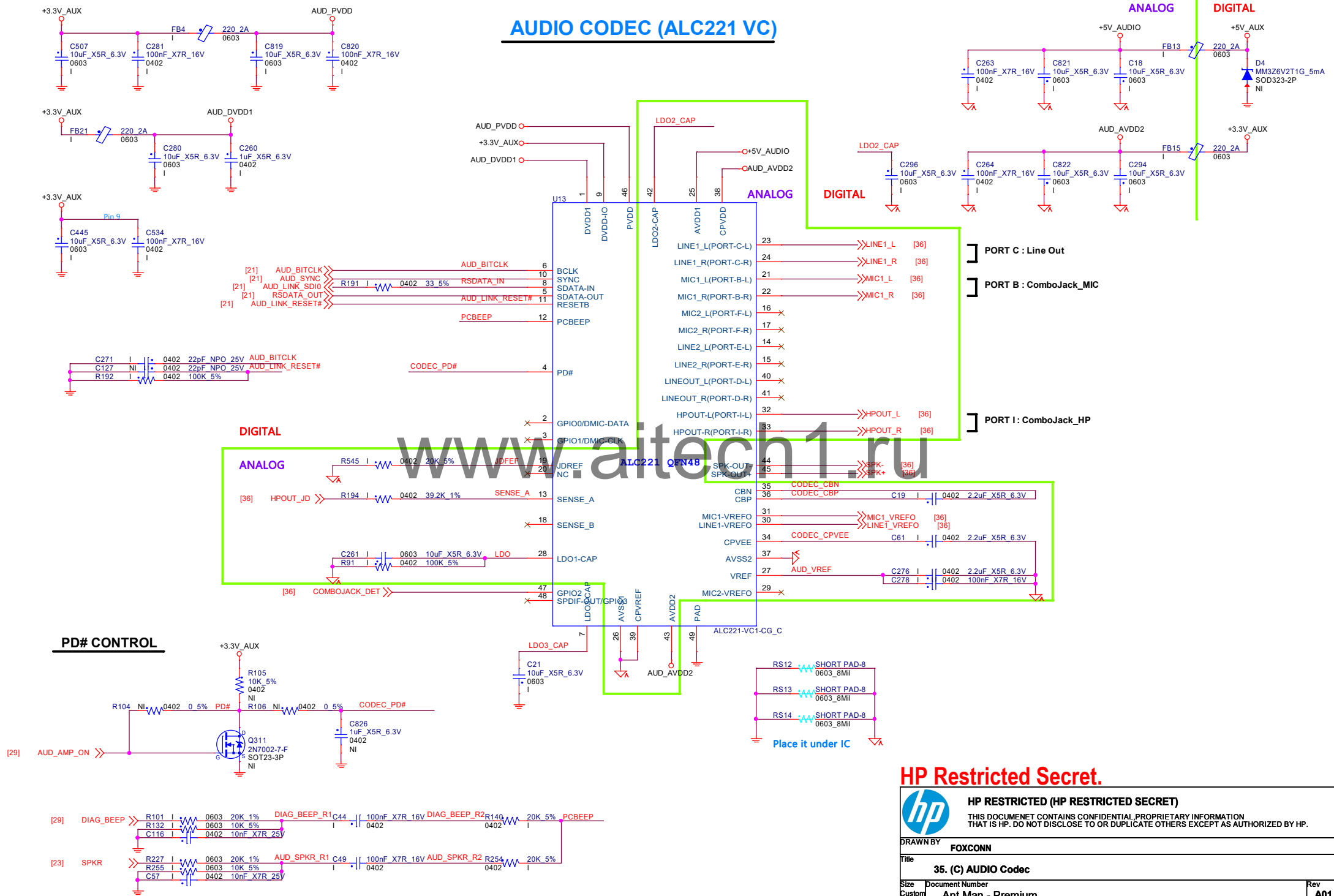
Remove P210

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		Title 34. (C) SATA	
Size Custom	Document Number Ant Man - Premium	Rev A01	
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AUDIO CODEC (ALC221 VC)



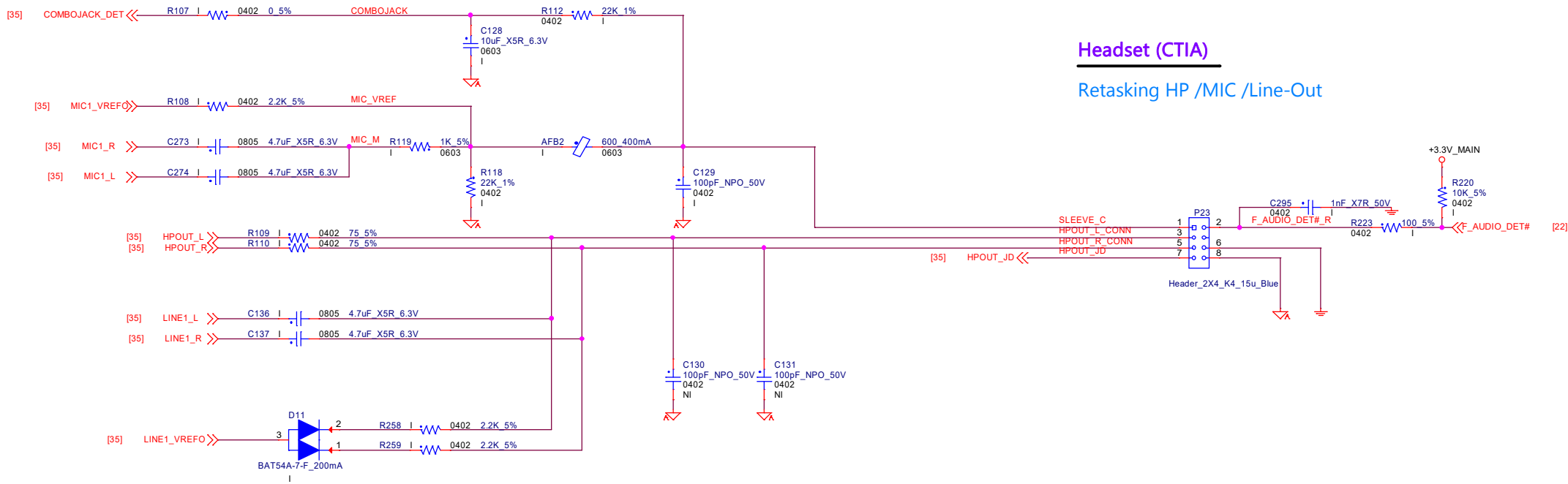
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Title: 35. (C) AUDIO Codec		Rev: A01	
Size: Custom	Document Number: Ant Man - Premium	Date: Wednesday, October 05, 2016	
Sheet: 35 of 98		Rev: A01	

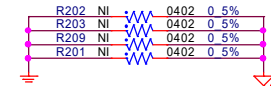
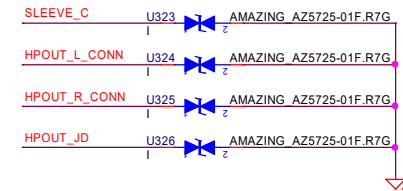
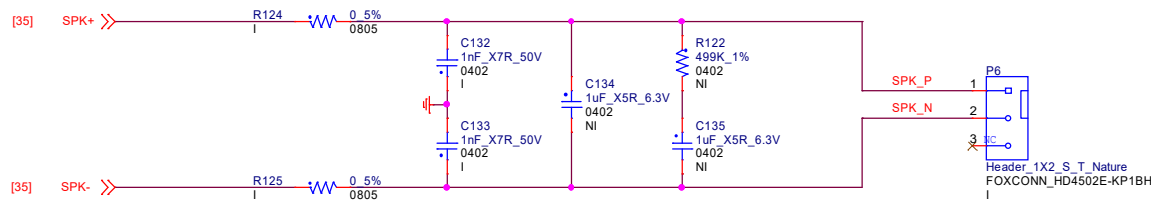
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Headset (CTIA)

Retasking HP /MIC /Line-Out

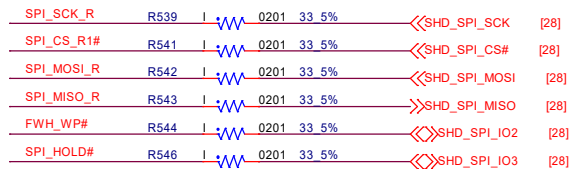


Speaker



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Size Custom	Document Number Ant Man - Premium	Rev A01	
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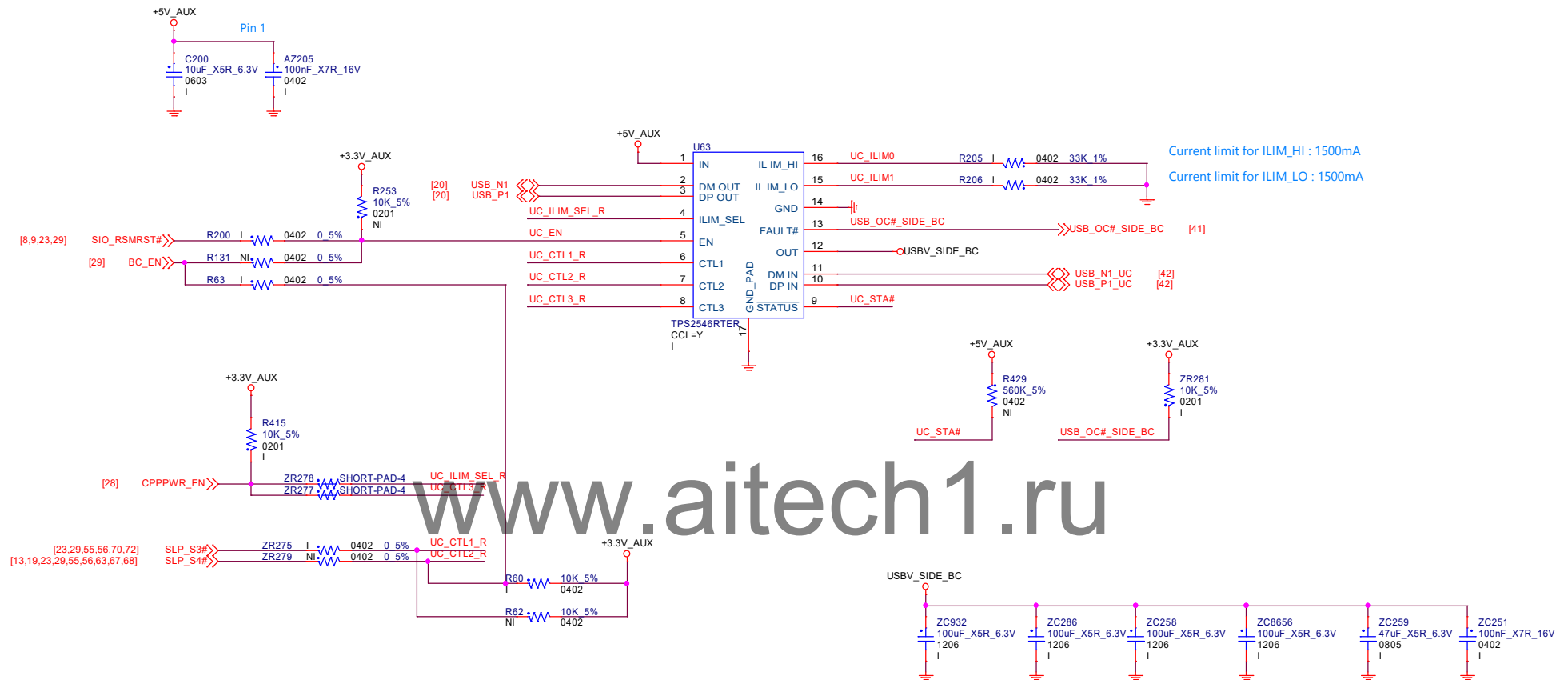
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USB Charging IC



USB Charging mode selection in System Status

Charging Port Function (Port Options in BIOS)	System State	CTL1 SLP_S3#	CTL2 BC_EN	CTL3 CPPPWR	ILIM_SEL CPPPWR	Charging Mode	ILIM	USB DATA	USB Wakeup
Enabled (Default)	S0	1	1	1	1	CDP	ILIM-Hi =1500mA	YES	N/A
Enabled (Default)	S3	0	1	1	1	DCP_Auto	ILIM-Hi =1500mA	NO	YES
Enabled (Default)	S4/S5	0	1	1	1	DCP_Auto	ILIM-Hi =1500mA	NO	YES
Disabled	S0	1	1	0	0	SDP	ILIM-Lo =1500mA	YES	N/A
Disabled	S3	0	1	0	0	SDP	ILIM-Lo =1500mA	YES	YES
Disabled	S4/S5	0	0	0	0	Discharge	N/A	NO	N/A

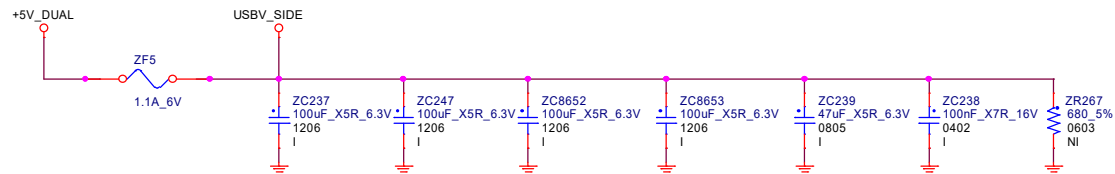
SDP : Standard Downstream Port
CDP : Charging Downstream Port
DCP : Dedicated Charging Port

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Title 40. (C) USB Charger			
Size	Document Number	Rev	
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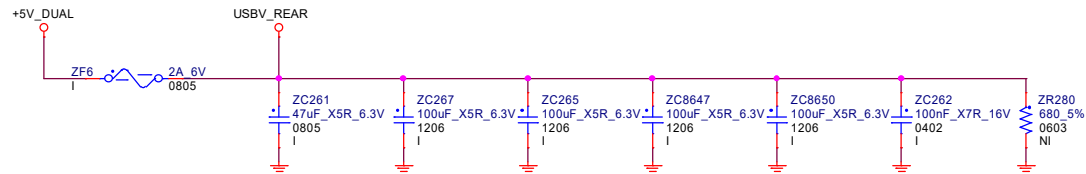
REAR USB POWER

SIDE : USB3*1

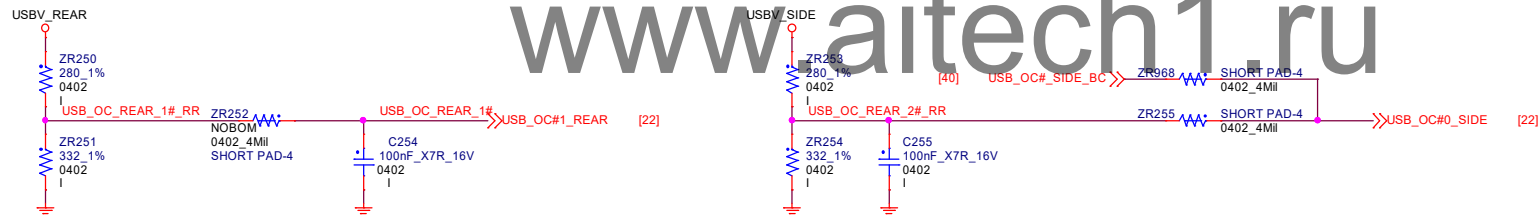


SIDE USB POWER

REAR : USB3*2



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41. (P)USB POWER

Size

Document Number

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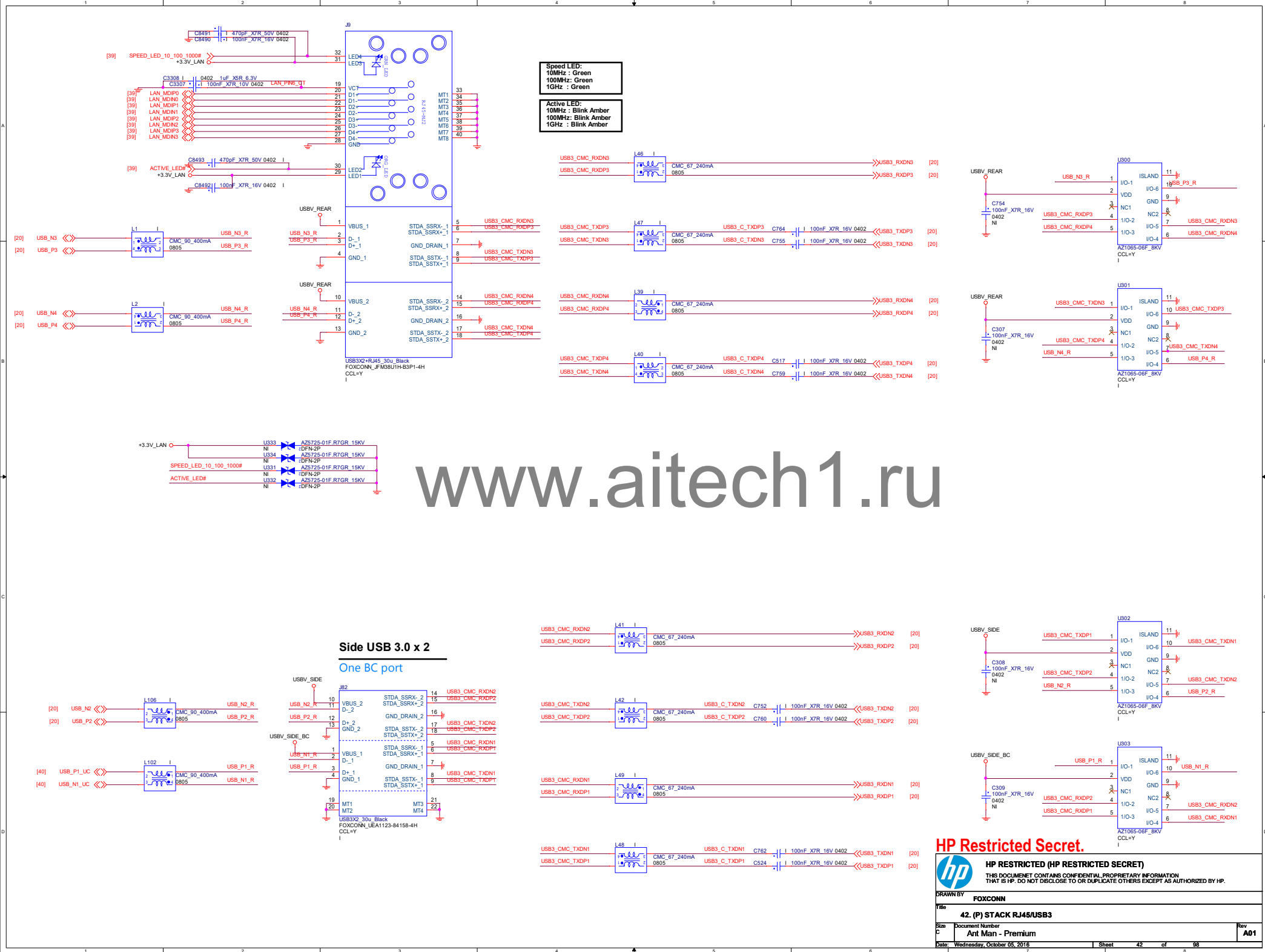
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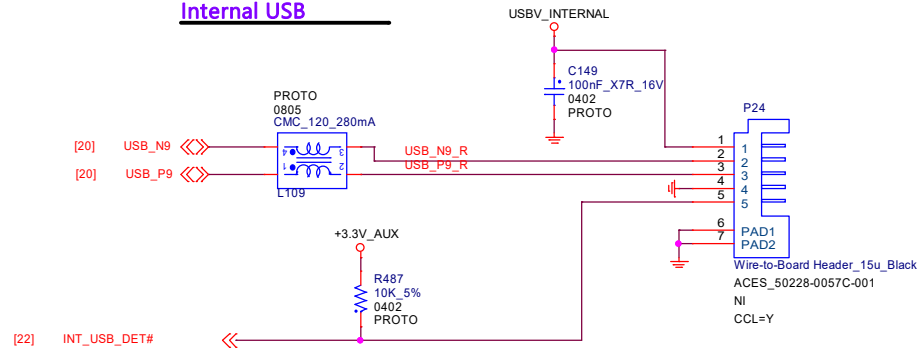
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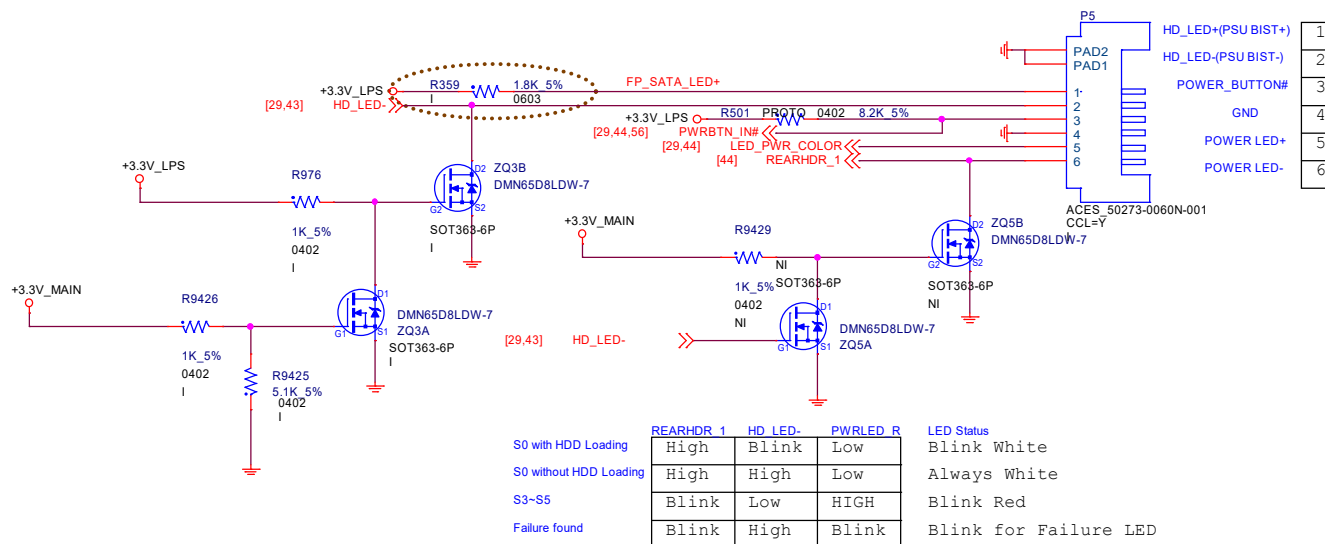


Internal USB



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Front Panel PWR BTN



S0 with HDD Loading
S0 without HDD Loading
S3-S5
Failure found

REARHDR_1	HD_LED-	PWRLED_R
High	Blink	Low
High	High	Low
Blink	Low	HIGH
Blink	High	Blink

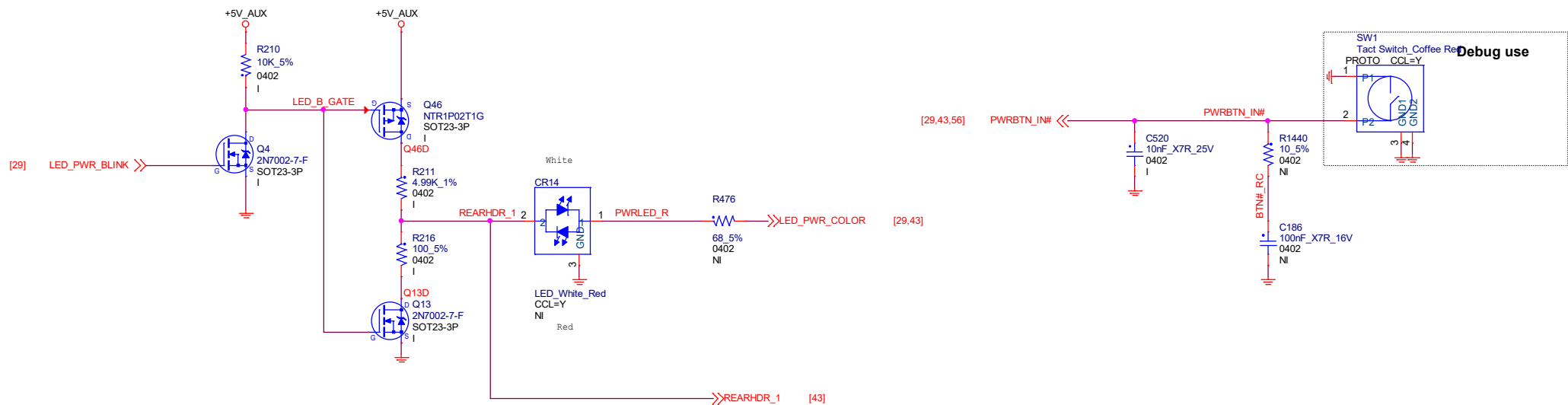
LED Status
Blink White
Always White
Blink Red
Blink for Failure LED

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Power Status LED

Power BUTTON



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44. (C) Power BTN

Size

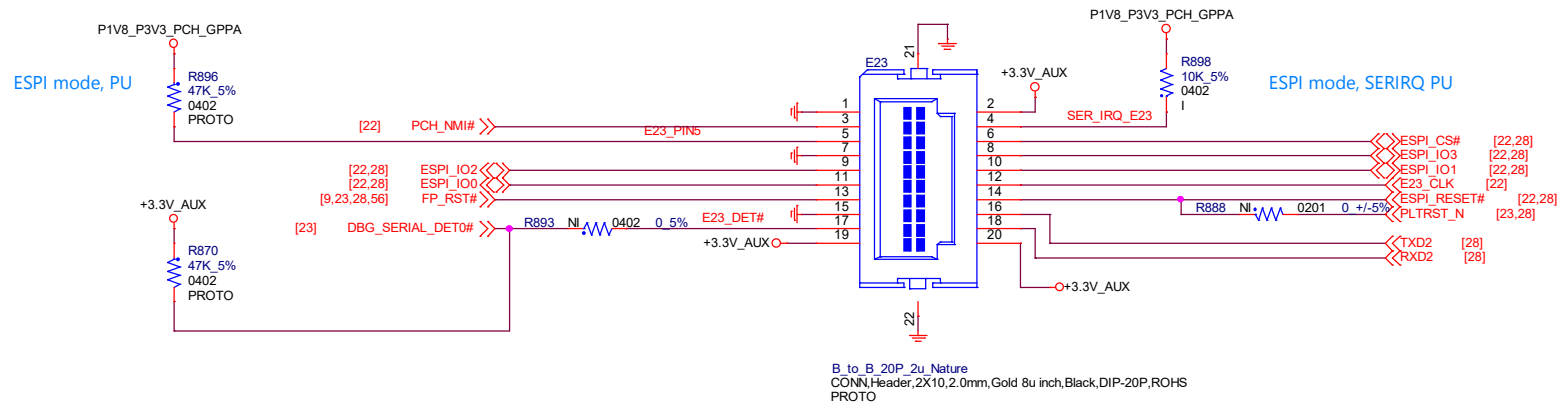
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PLATFORM DEBUG HEADER

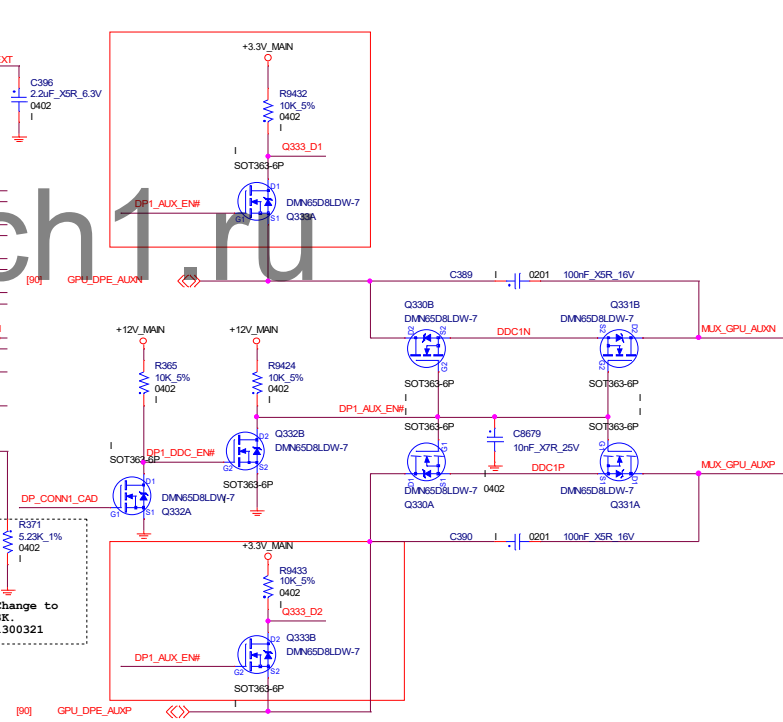
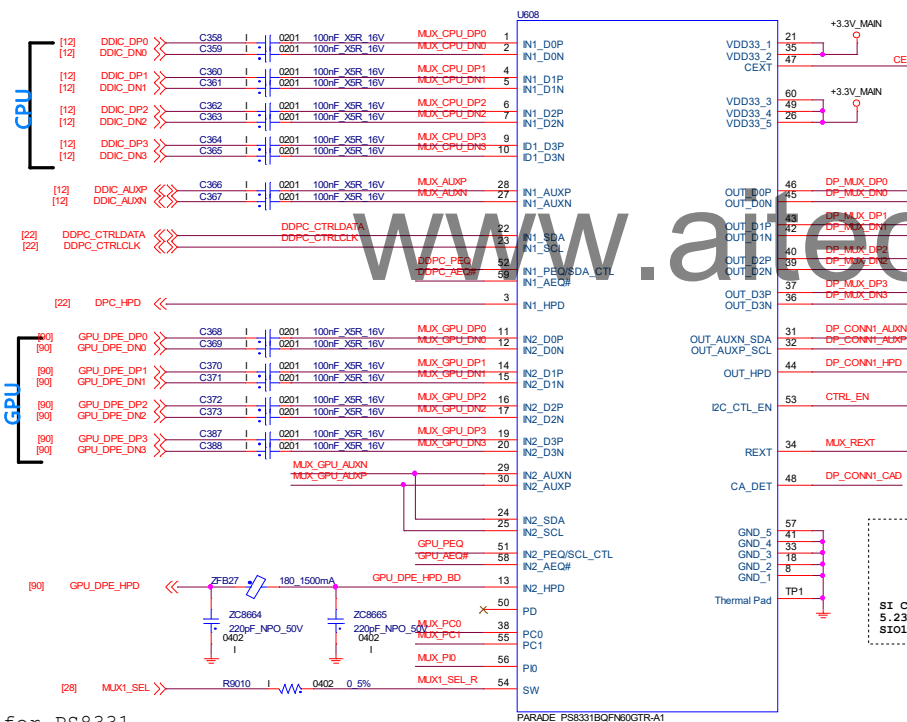
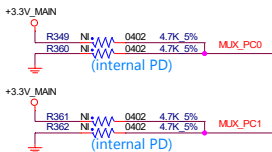
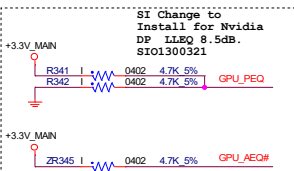
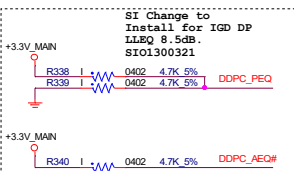
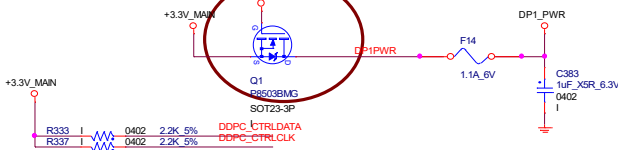
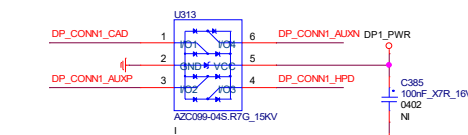
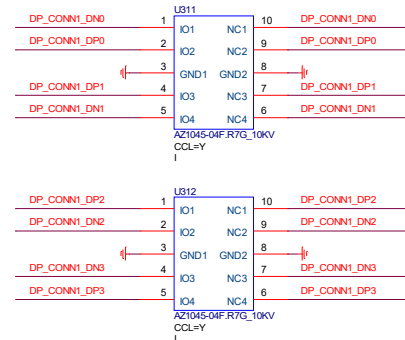
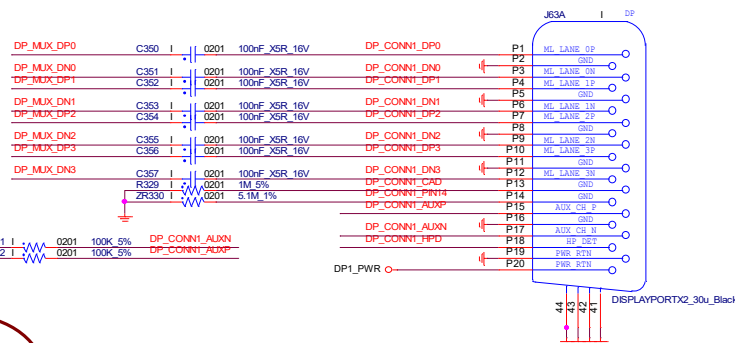


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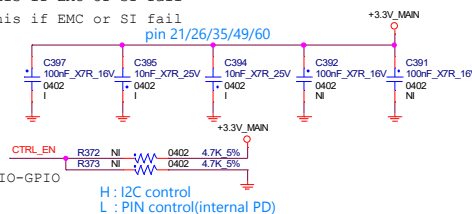
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DisplayPort #4 (Mux with CPU)



GPIO for PS8331

PCA_ID	H	NOTE	L	NOTE	M	NOTE	
GPU_PEQ	10K	14.5dB	NI	11.5dB	NI	8.5dB	Internal PD
DDPC_PEQ	10K	14.5dB	NI	11.5dB	NI	8.5dB	Internal PD
DDPC_AEQ#	NI	EQ-DIS	NI	EQ-EN	NA	NA	Internal PD
GPU_AEQ#	NI	EQ-DIS	NI	EQ-EN	NA	NA	Internal PD
CTRL_EN	NI	I2C	NI	PIN	NI	I2C	Internal PD
MUX_PIO	NI	TEST-EN	NI	TEST-DIS	NI	OFFSET-DIS	Internal PD
MUX_PC0	NI	AUX-INT-DIS	NI	AUX-INT-EN	NI	AUX-INT-DIS	Internal PD
MUX_PC1	NI	+20%	NI	Default	10K	-16.7%	Internal PD SWING
MUX1_SEL_R	NI	Port2	NI	Port1	NA	NA	Internal PD
PD	NC	PWR-OFF	NC	Normal	NA	NA	Internal PD



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46. (P) DP4 (MUX WITH CPU)

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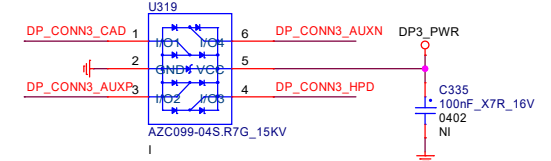
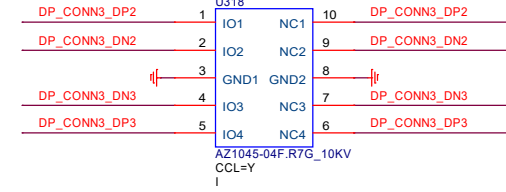
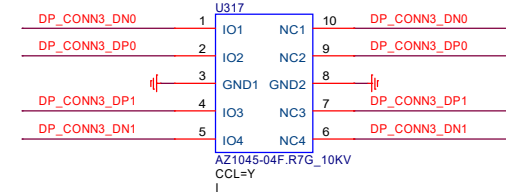
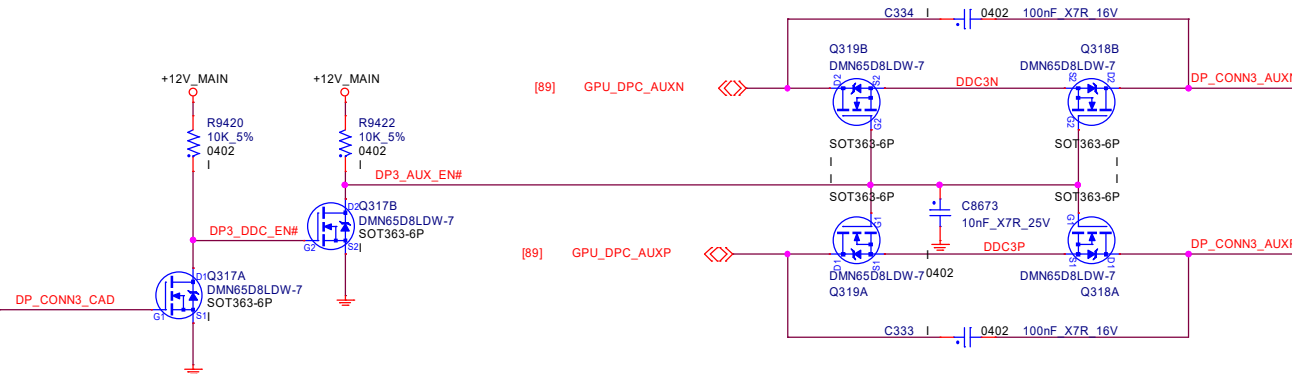
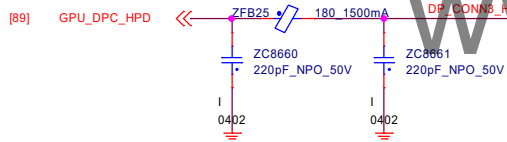
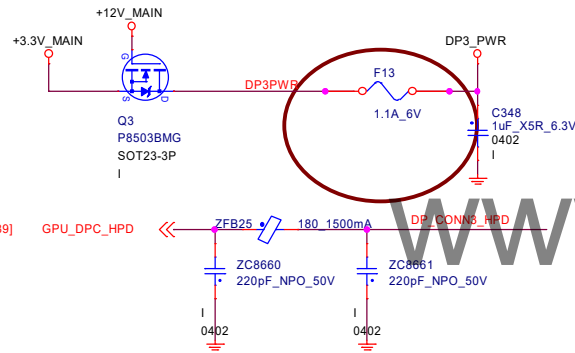
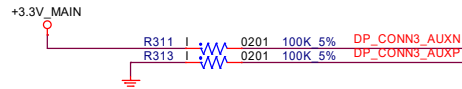
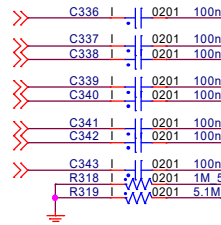
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DisplayPort #2

GPU Port C

[89] GPU_DPC_DP0
[89] GPU_DPC_DN0
[89] GPU_DPC_DP1
[89] GPU_DPC_DN1
[89] GPU_DPC_DP2
[89] GPU_DPC_DN2
[89] GPU_DPC_DP3
[89] GPU_DPC_DN3

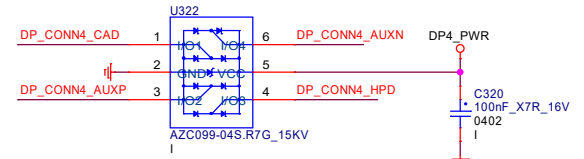
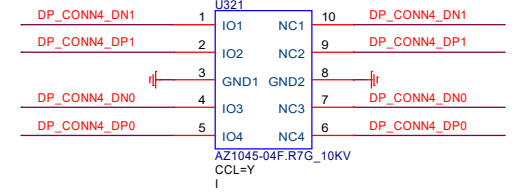
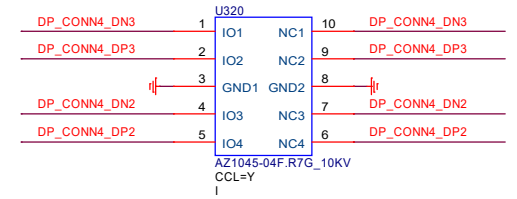
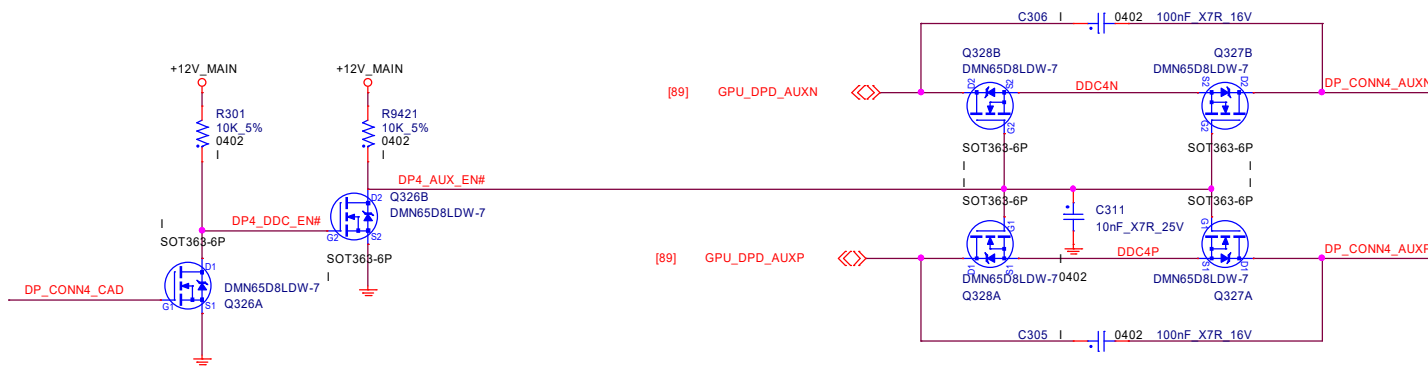
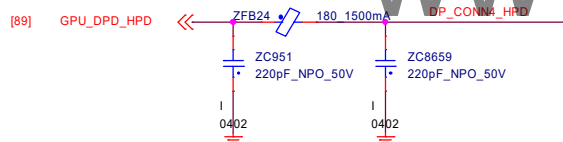
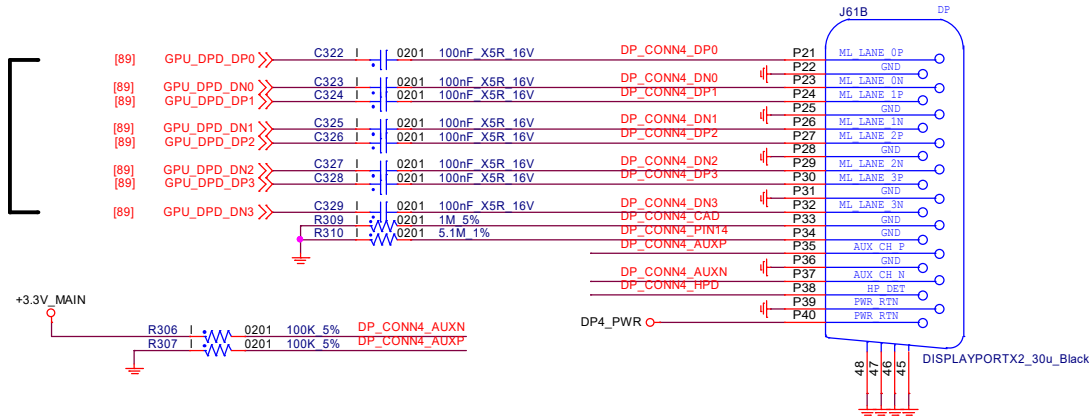


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DisplayPort #1

GPU Port D




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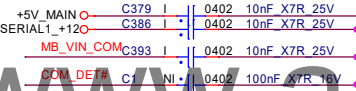
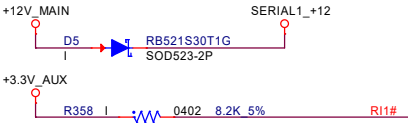
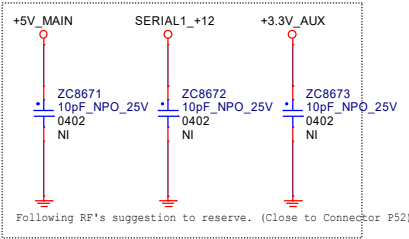
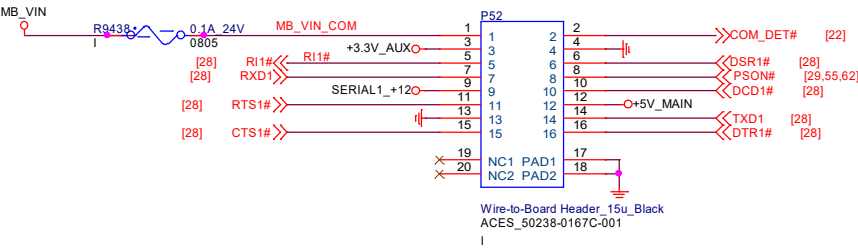
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SERIAL Port Header



P52

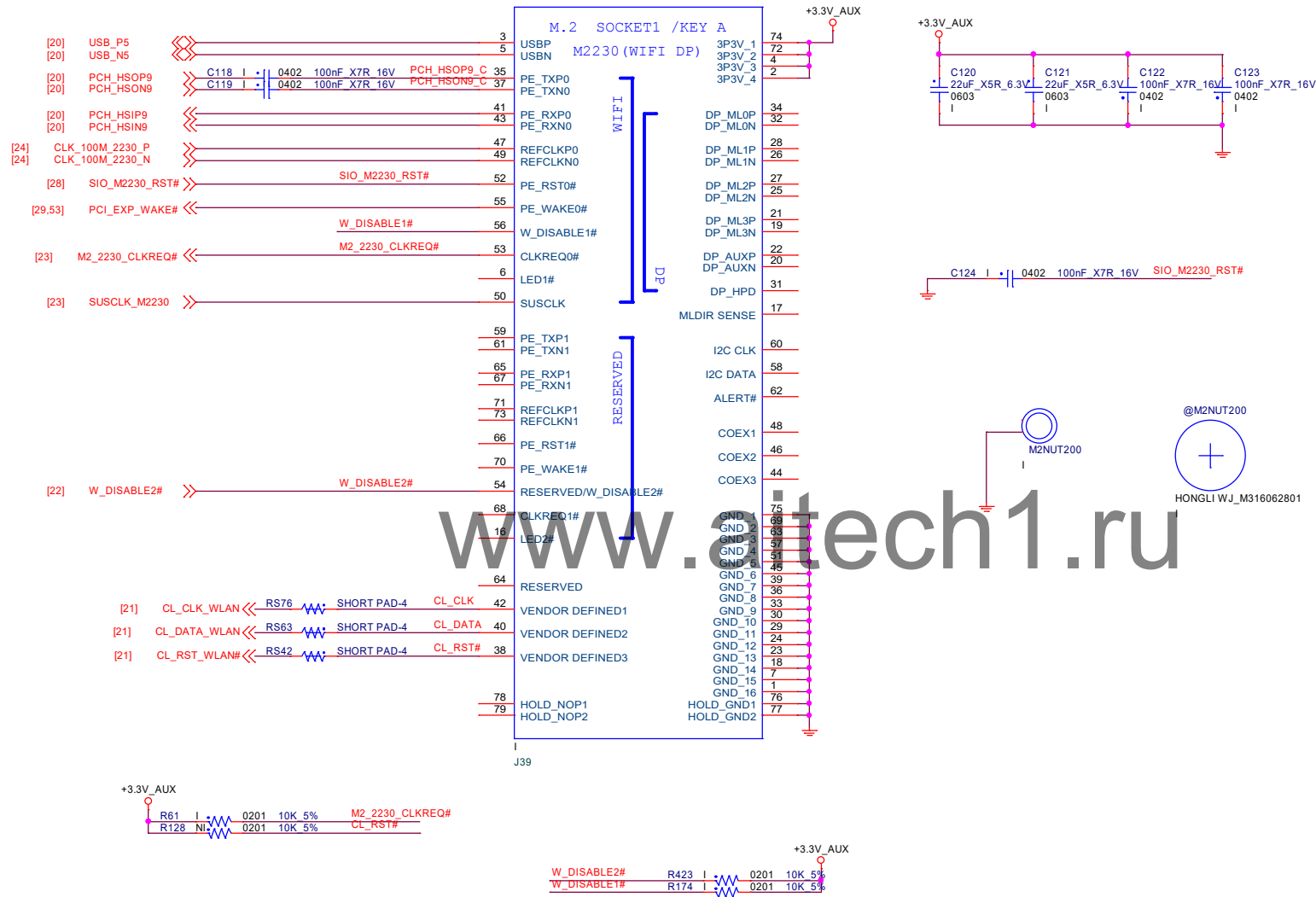
Serial B

1	COM_DTR2#	2	COM_SDIN2
3	COM_CTS2#	4	COM_DSR2#
5	COM_SD02	6	COM_R12#
7	GND	8	GND
9	+5V_SYS	10	+3.3V_SB
11	COM_RTS2#	12	COM_DET#
13	COM_DCD2#	14	+12V_SYS
16	+12V_SYS	16	KEY

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Size	Document Number	Rev	
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Date:	Wednesday, October 05, 2016	Sheet	51 of 98

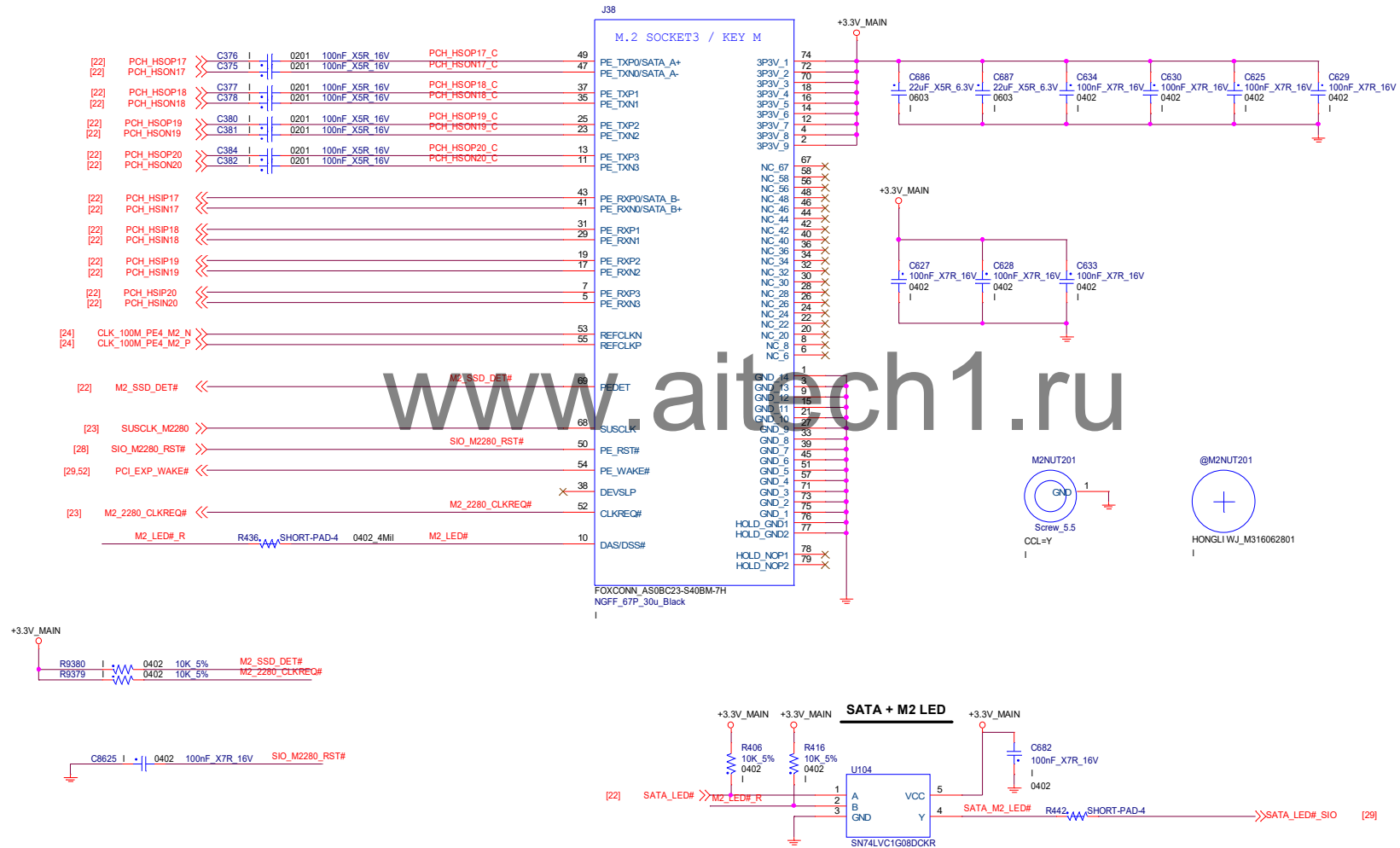
M2. 2230 Key A - WLAN



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Size: Custom	Document Number: Ant Man - Premium	Rev: A01	
Date: Wednesday, October 05, 2016		Sheet: 52	of: 98

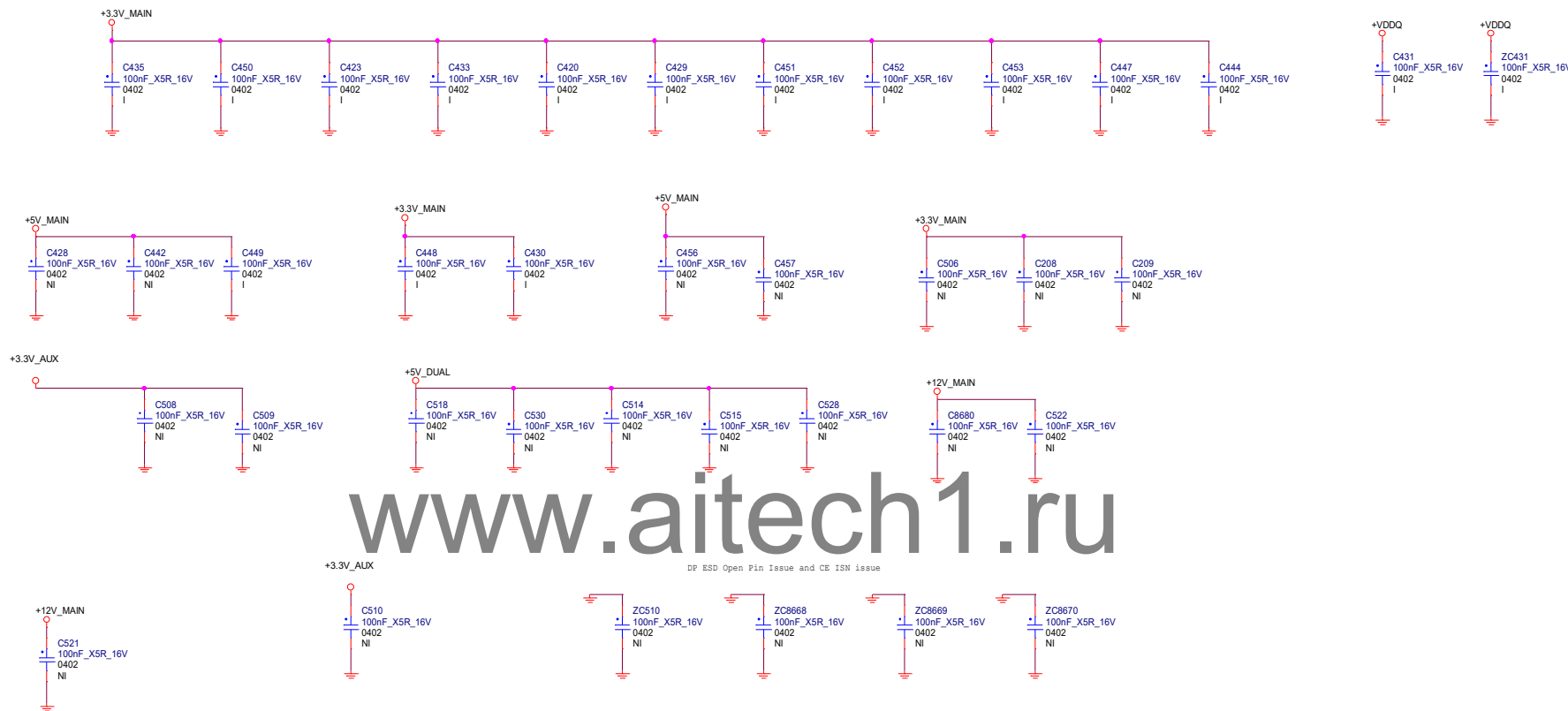
M2. 2280 - STORAGE



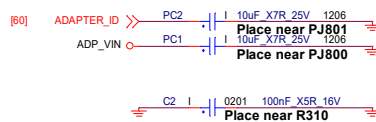
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Size: Custom	Document Number: Ant Man - Premium	Rev: A01	
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EMI CAP



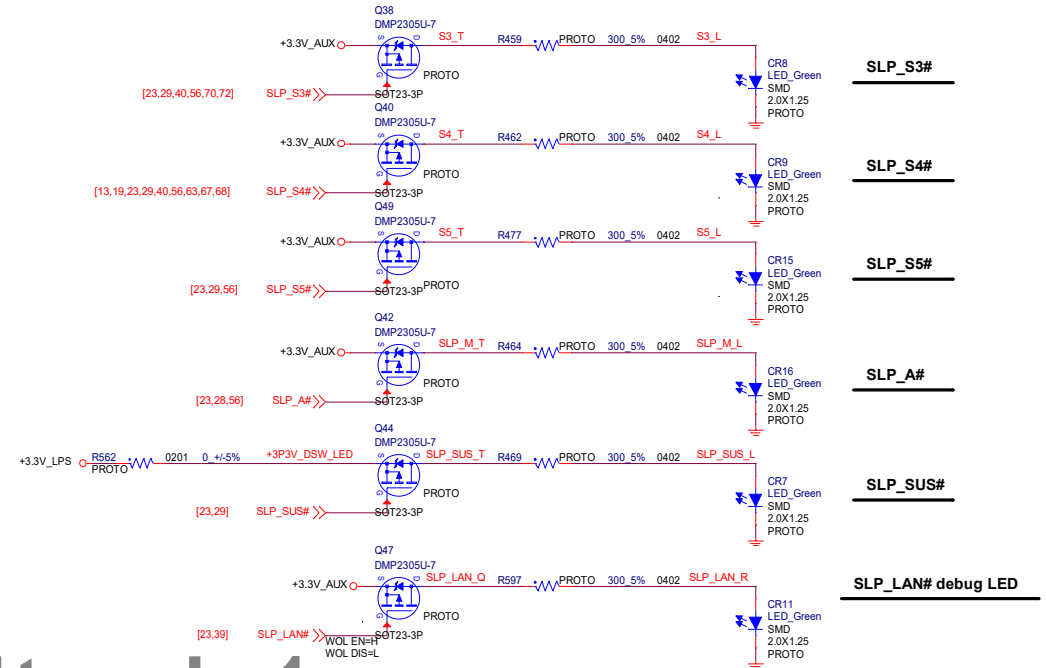
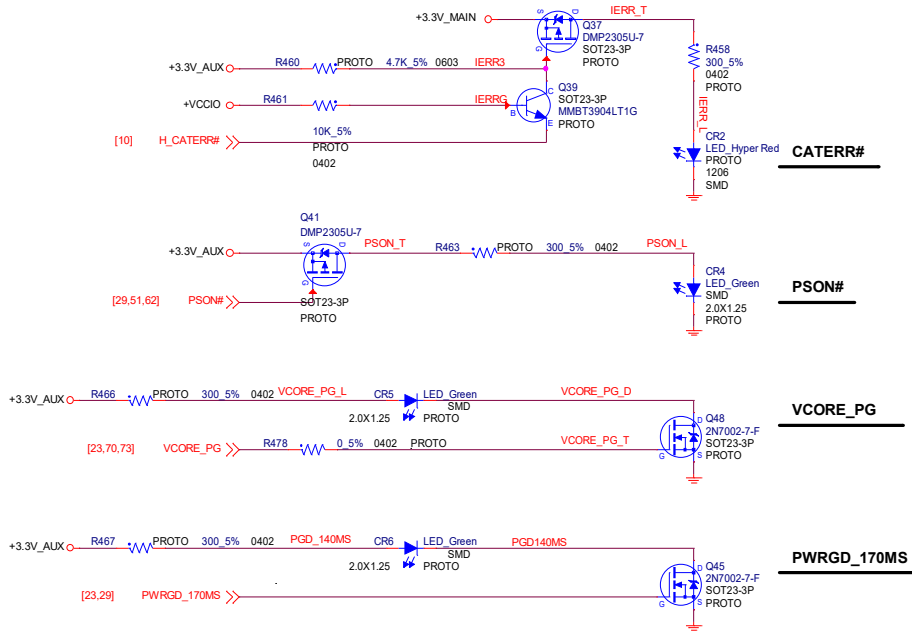
Add on Si1



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Title		54. (C) EMI CAP	
Size	Document Number	Rev	
Custom	Ant Man - Premium	A01	
Date: Wednesday, October 05, 2016		Sheet	54 of 98

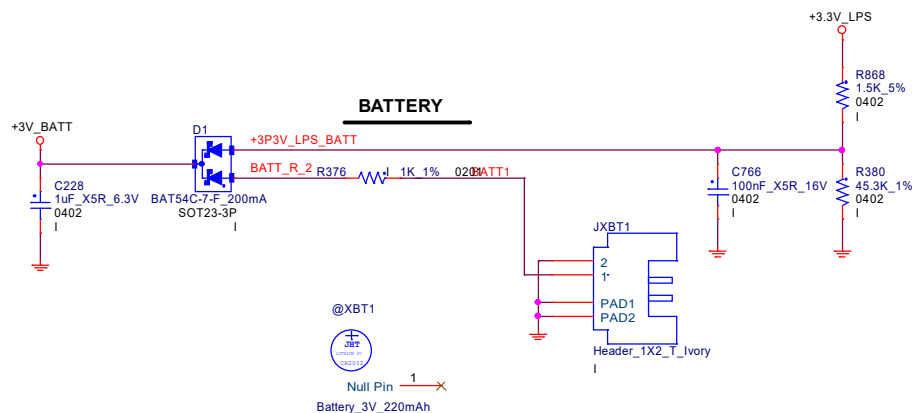
PCA LEDs



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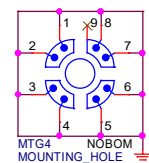
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		DRAWN BY: FOXCONN	
Title: 55. (C) Debug LEDs		Size: Custom	
Document Number: Ant Man - Premium		Rev: A01	
Date: Wednesday, October 05, 2016		Sheet: 55 of 98	



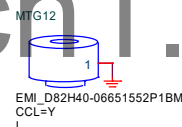
PCB1
Printed
Circuit
Board

PCB_REV:1.01
CCL=Y
8-Layer PCB,Color With Dark Blue Soldermask,White Silkscreen,EM-285,ML1,7.9x7.9 inch,Rev:1.01,ROHS,HF
0101DCS06-35K-H

Screw hole for Premium (left-upper corner)
HDD CAGE STAND OFF

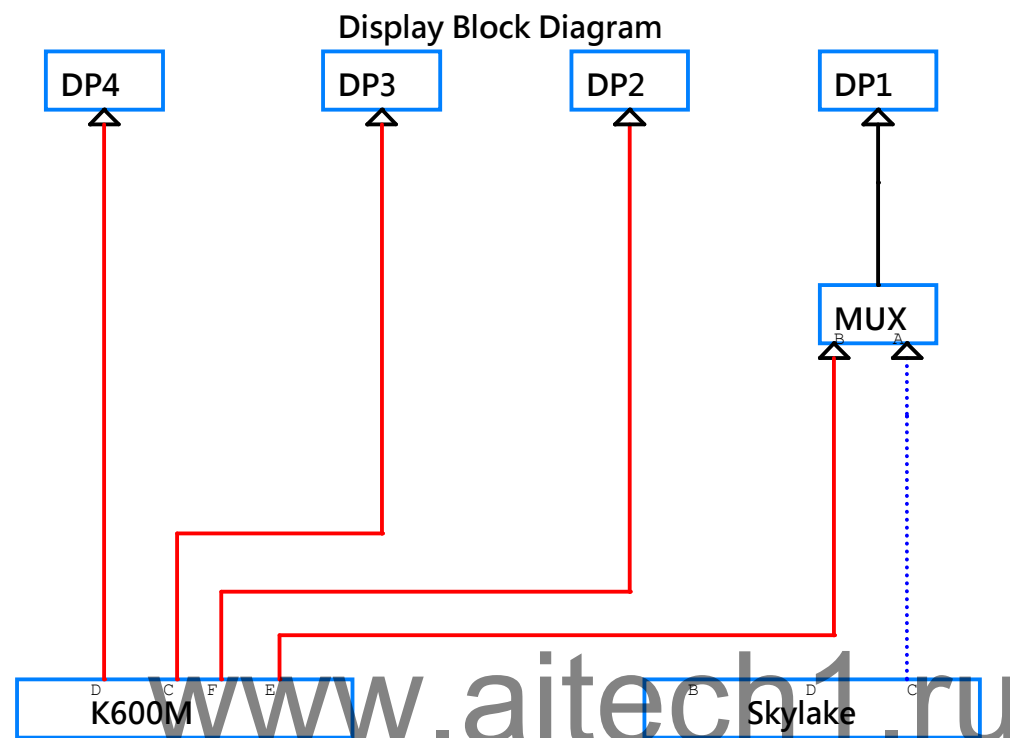


Screw hole for Premium (left-down corner)
GPU STAND OFF




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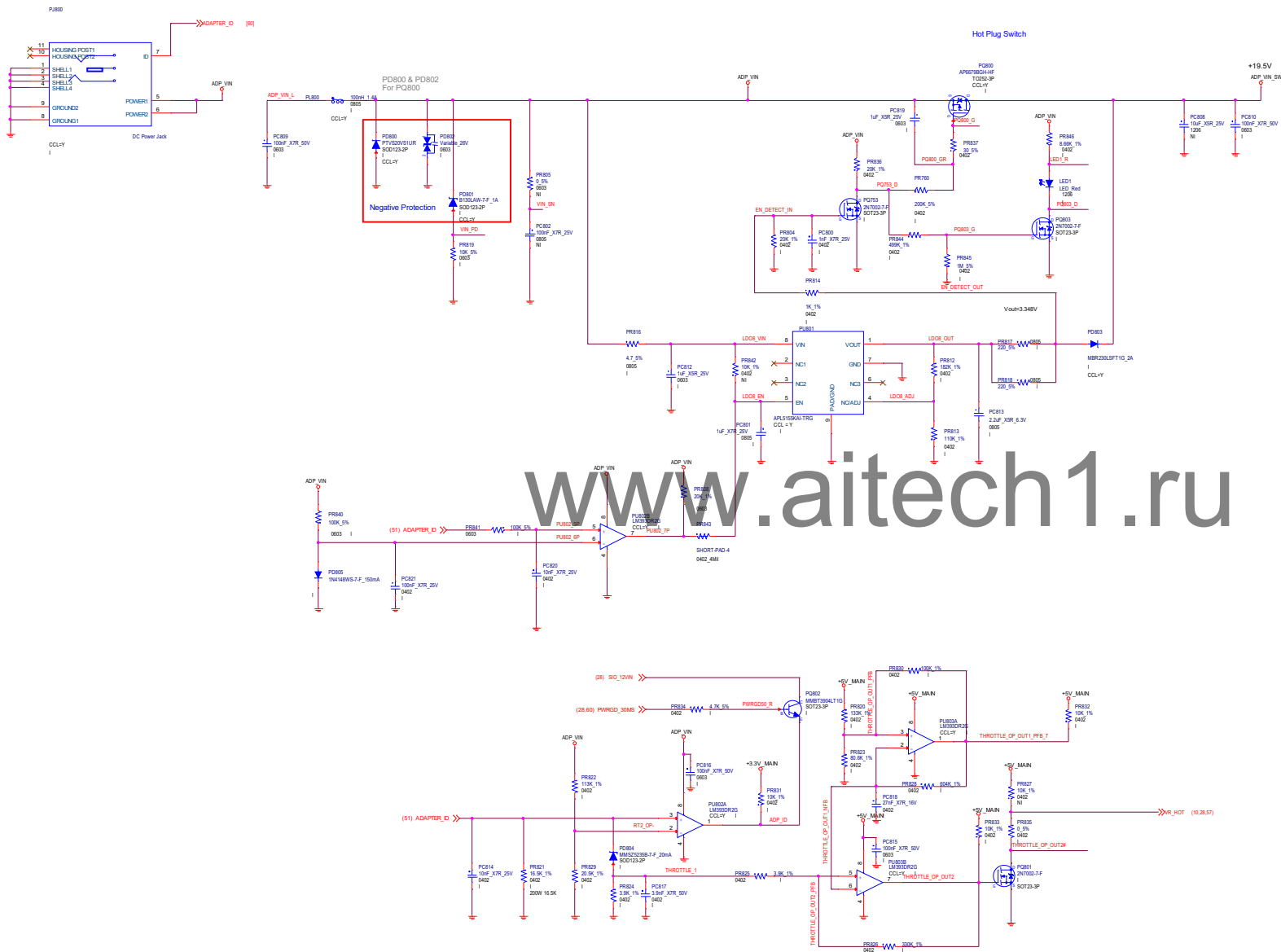
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Title		58. (P)Display Block Diagram	
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19V DC Power Adapter-in



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File

Adapter IN

Size

Document Number

Content

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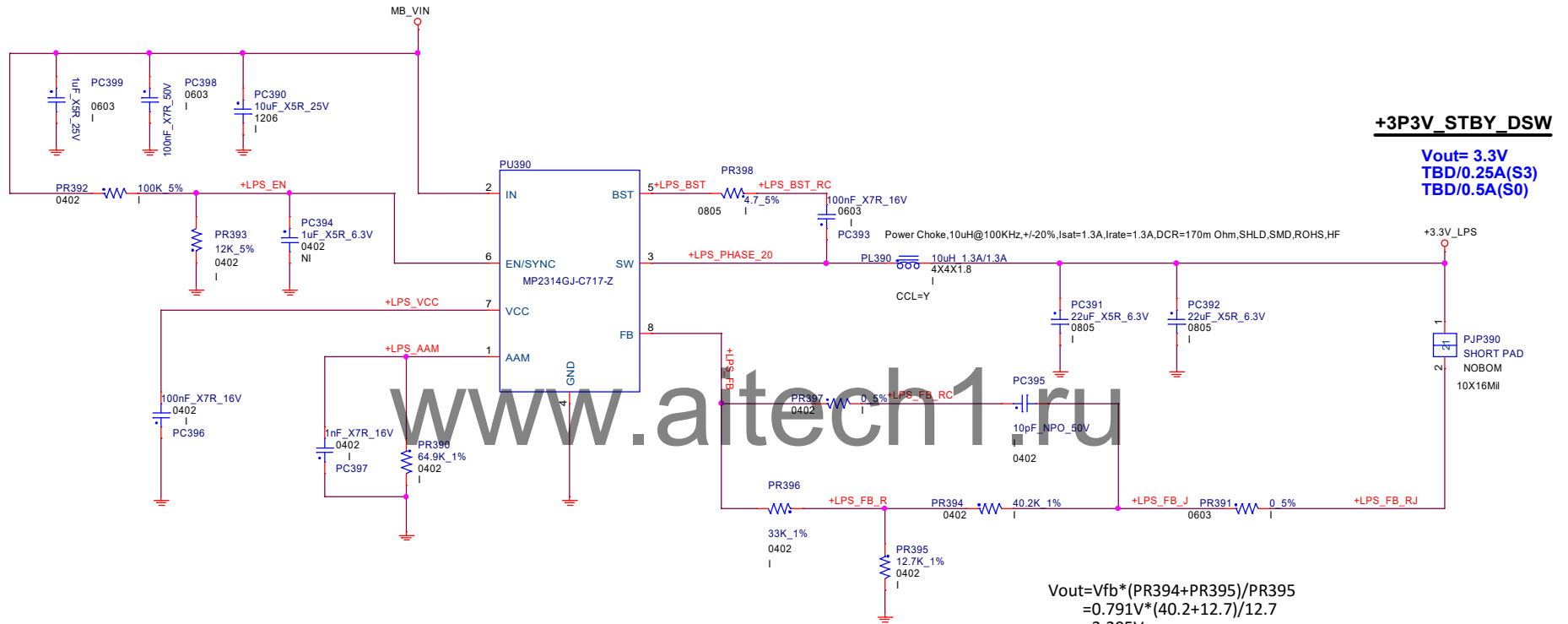
Date

Revision: 0.01.01.01

Rev

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+3P3V LPS



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Title

+3.3V_LPS

Size

Custom

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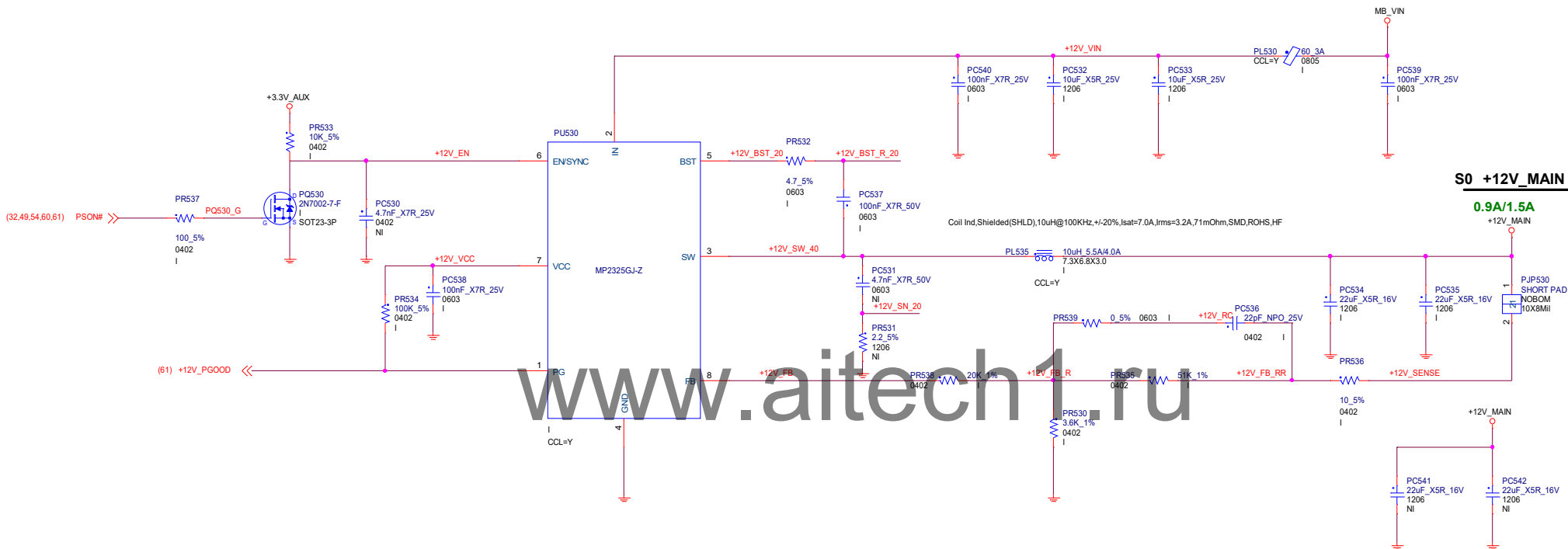
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Note: net-name:Switch1



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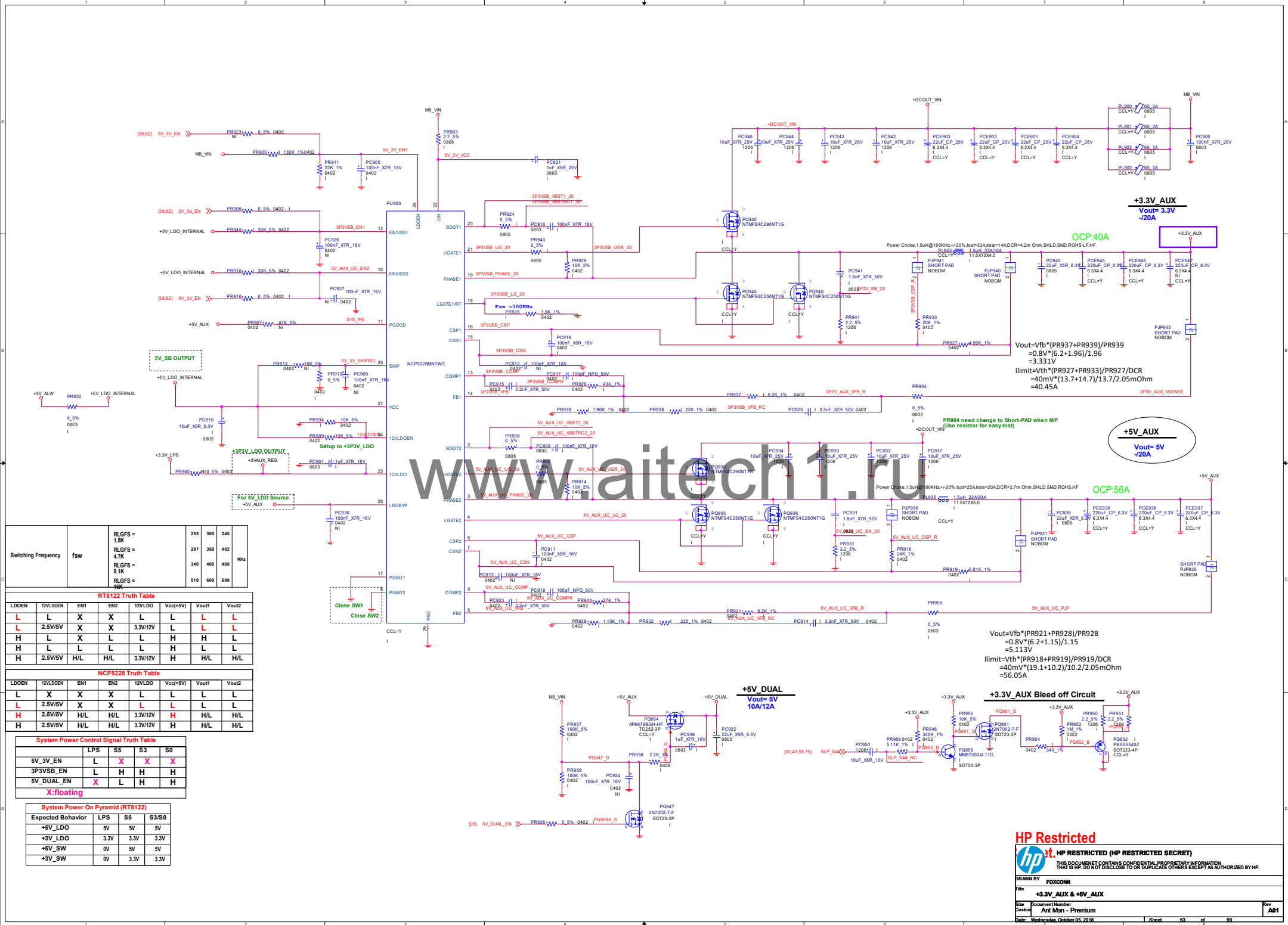
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Size	Document Number
Custom	Ant Man - Premium

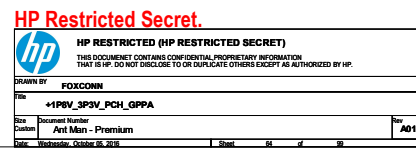
Date: Wednesday, October 05, 2016

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Date:	Wednesday, October 05, 2016	Sheet	62	of	99
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Size
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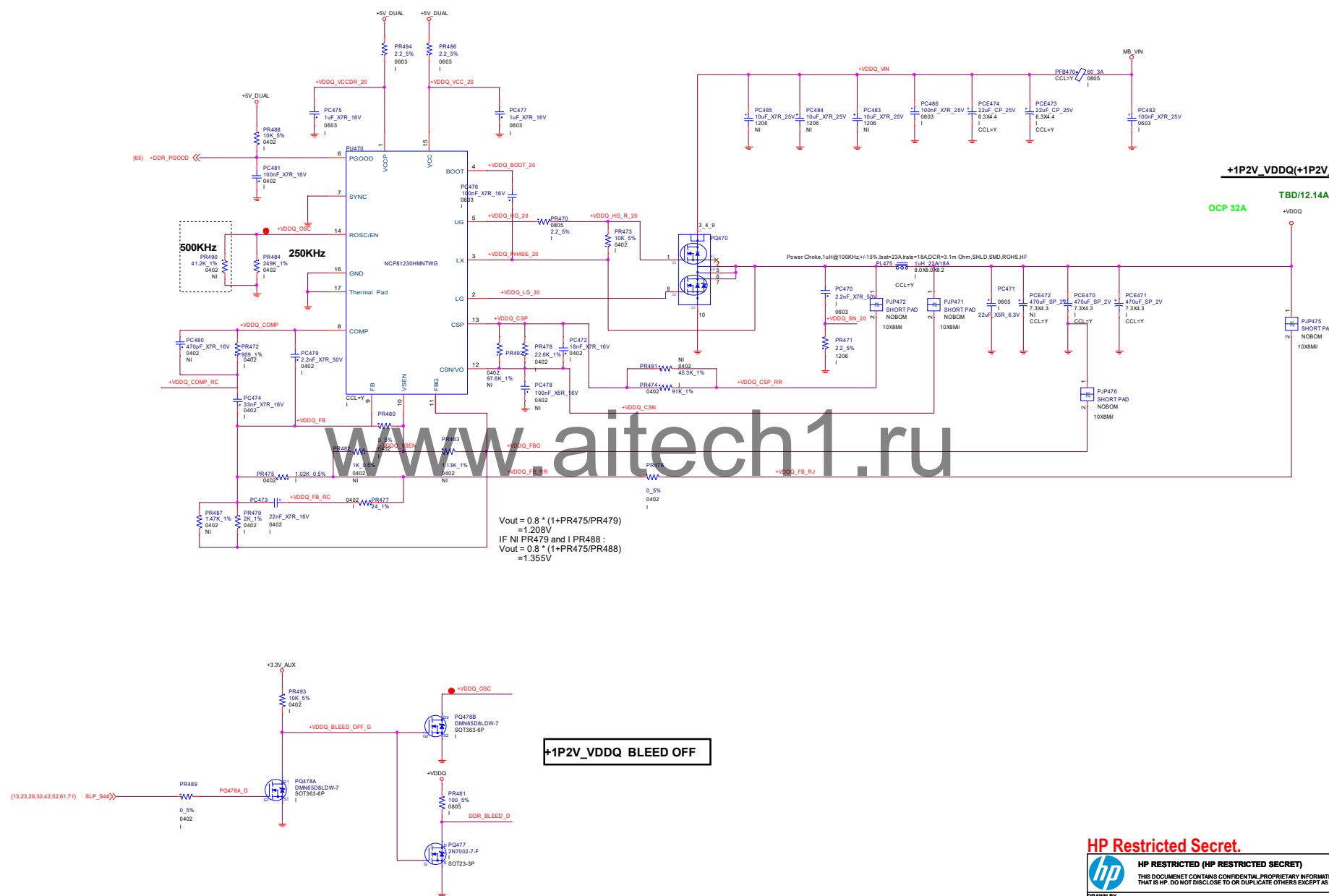
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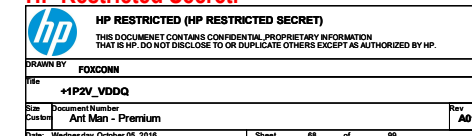
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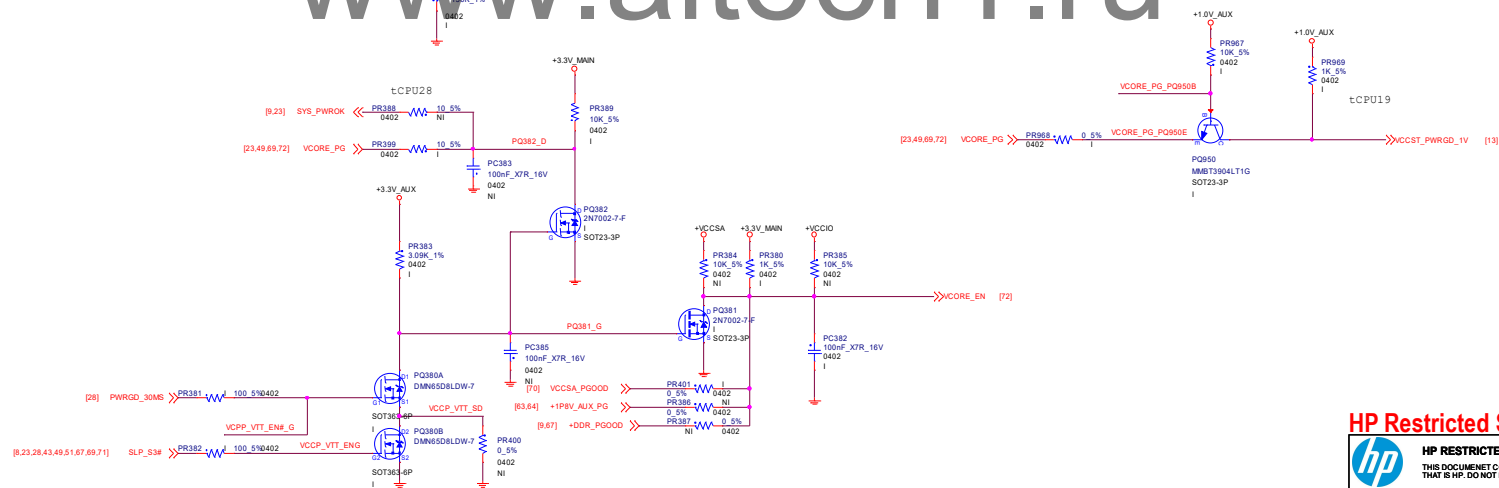
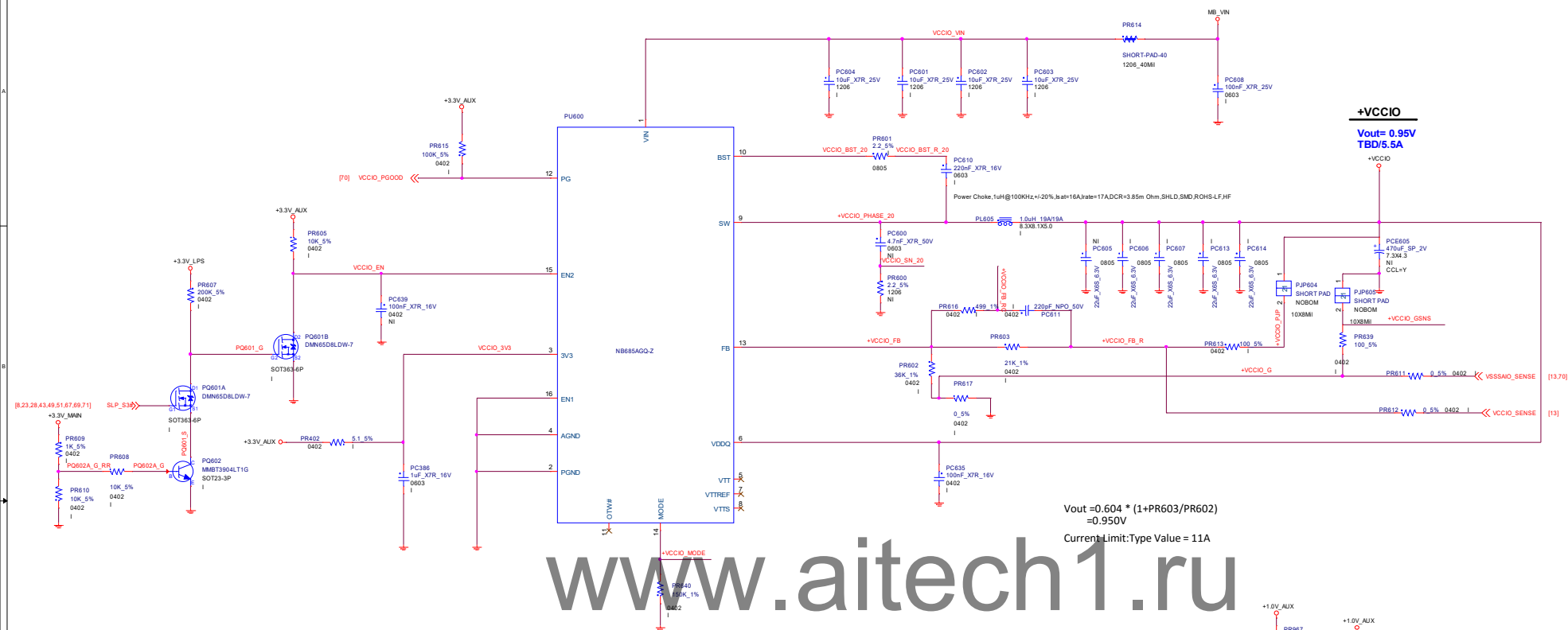
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+1P2V_VDDQ

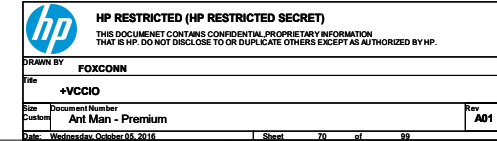


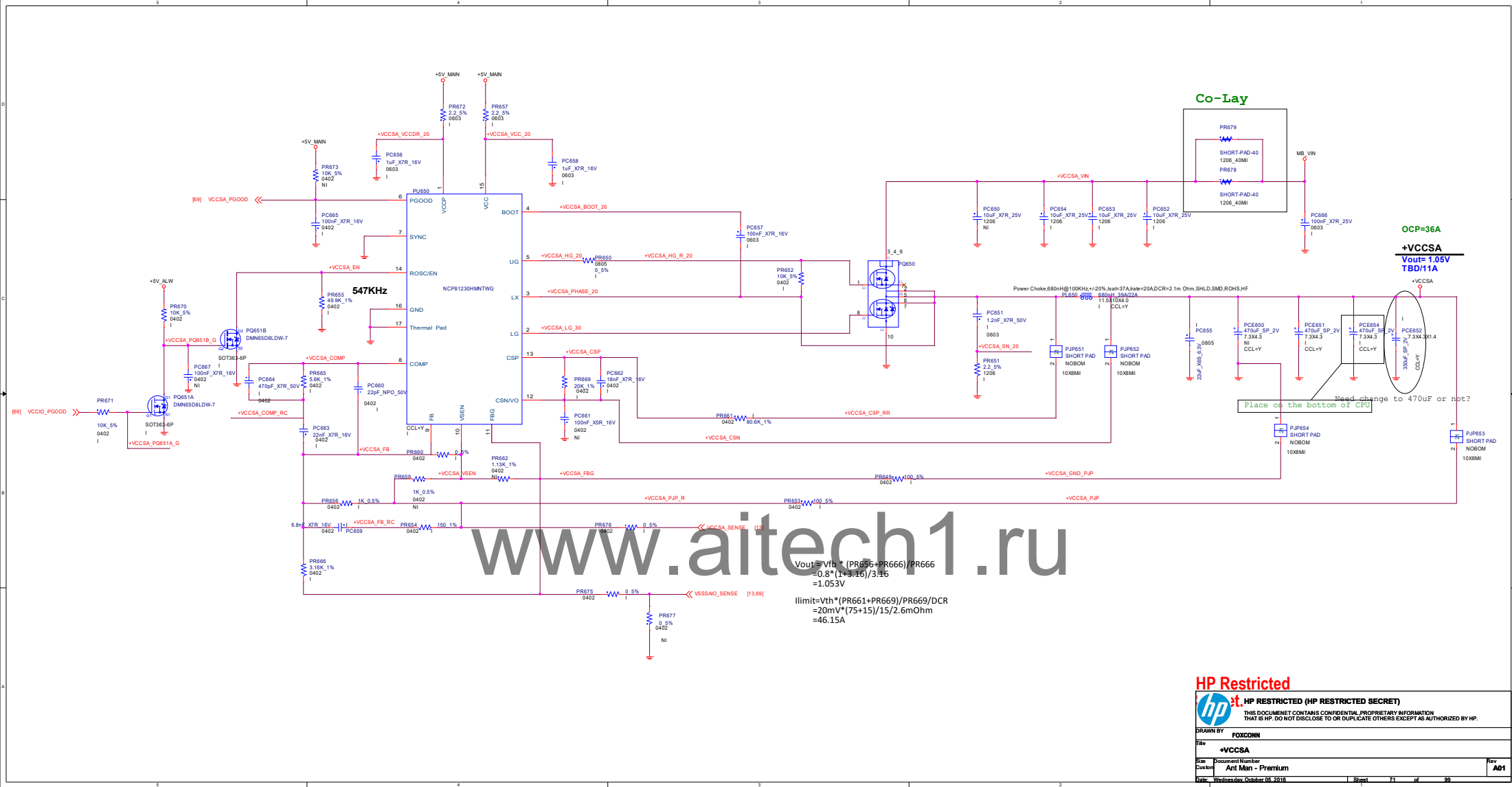
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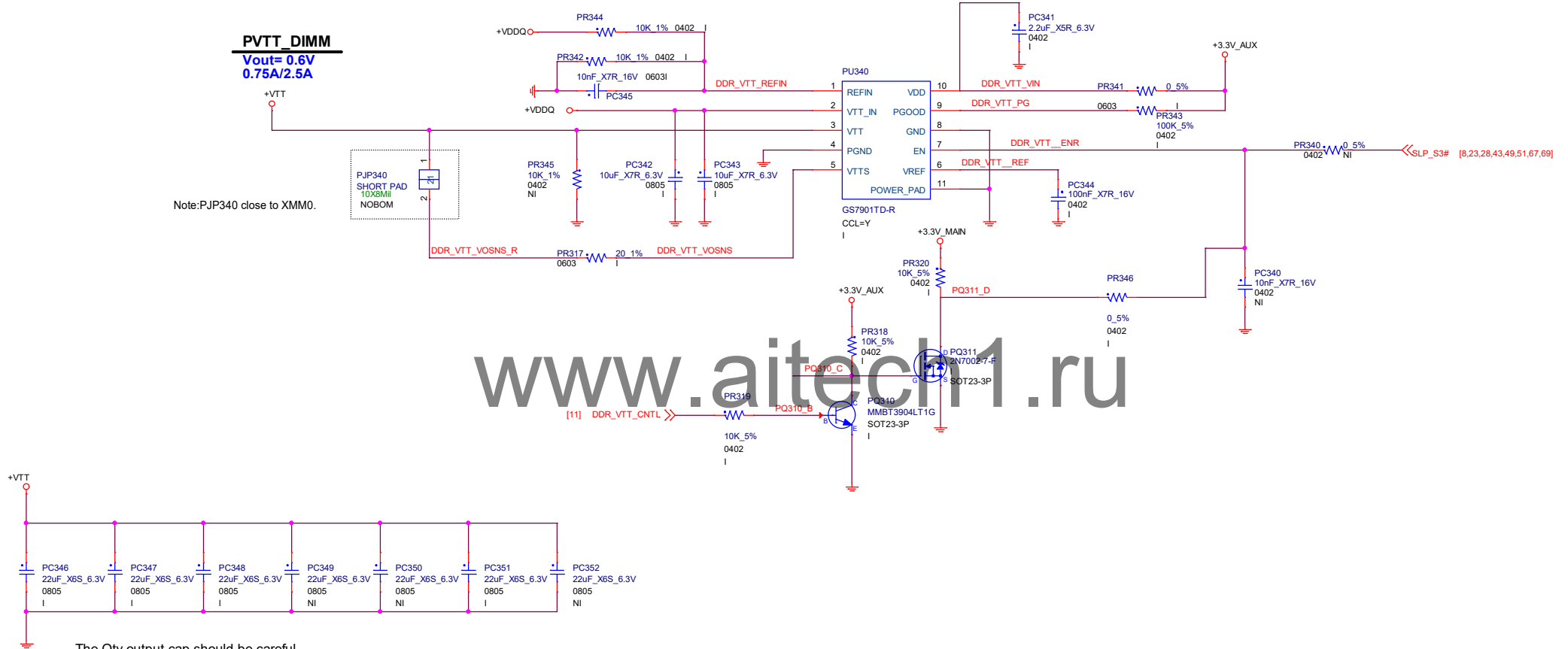


DDR_VTT

PVTT_DIMM

Vout= 0.6V
0.75A/2.5A

Note:PJP340 close to XMM0.

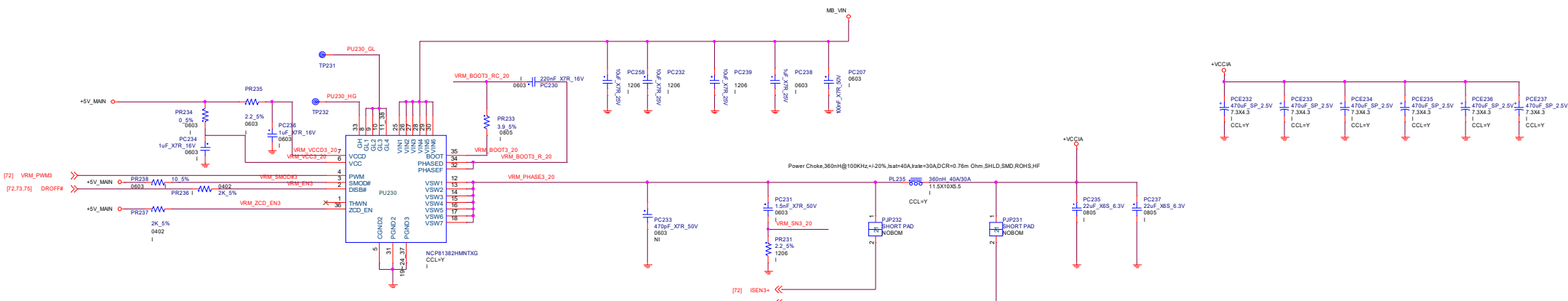


The Qty output cap should be careful
INTEL: the latest modeling shows step load size 6-9x higher than it's shown in PDG
1.0 for Aztec City CRB

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VCORE PHASE3



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+VCORE PHASE3

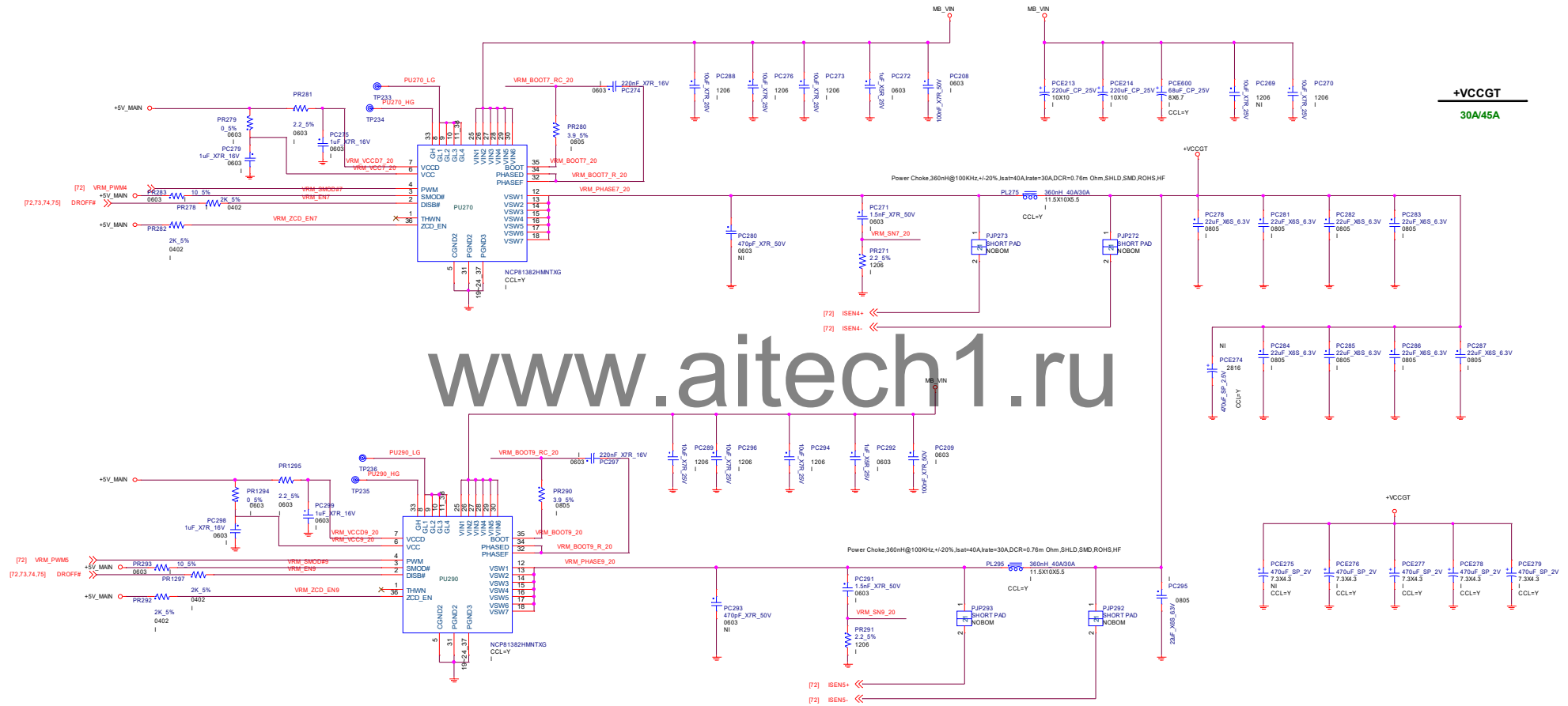
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VCCGT PHASE1&2



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File	+VCCGT PHASE 1 & 2	
Doc	Document Number	
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Rev
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ITEM	DATE	CHANGE (REF: 3510250054)
		FOR: B1
20160419		1. Page 96 PWM3 change from 1 to NI, PWM8554 from NI to 1, to adjust NVidia W800R power sequence; S10128702
20160426		1. Page 60 Change PR821 from 14.3k, 1% to 16.5k, 1%, due to the entry adapter is 200R; S101289118 2. Change PR8673 from 1 to NI, It double pull high S101289131
20160520		1. Page 75 Change PC2323*PC2327 change from EEP3510471E4 to EEP3510647184; S101290564
20160524		1. Page 73 Changes is below: PR132 to 215k, 1%, PC122 to 2.2nf, PC123 to 680pf, PR103 to 32.4k, 1%, PR135 to 2.28k, 1%, PR124 to 2.28k, 1%, this solution for VBIT test; S101290538
		2. Page 74, 75 Change PC211, PC221, PC231 to 3.3nf, VTR_50V, to fix number RES thermal issue; S101296331
		3. Page 97 change PWM562 to 0603 size; S101296331
		4. Page 99 change PWM343 to 0603 size, add PWM602 0.5u; S101296331
		5. Page 98 change PWM321, PWM324 to 0603 size, PWM329 net change to NVYD0_V1N; S101296331
		6. Page 65 change PR520 to 1.24k, 1%, PR522 to 49.9ohm, 1%; S101297339
		7. Page 68 change PC474 to 33nf, PR472 to 909ohm, 1%; S101294178
		8. Page 71 change PR855 to 49.9k, 1%; S101297335
		9. Page 71 change PC222, PC238 to X7R; S101290564
20160506		1. Page 98 change PWM321, PWM324 from 330pf to 2.2nf to reduce the LS Vdc; S101296331
20160531		1. Page 98 Add PWM713, PWM714 470pf 0603 size to reduce the LS Vdc; PWM506, PWM334 to 1.5n 0805 size; Change PWM504 from 0.5u to 100nf, 1%, to adjust VTR power rail; S101298988
		2. Page 99 Change PWM343 from 1.0nf to 2.2nf, PWM503 from 0ohm to 2.2 ohm; S1014500403
20160606		1. Page 60 change FB002 change from INPA_MU3Y0603K20 to INPA_MU3Y0603K20, because of different POC.
20160621		1. Page 98 PWM854 suggest set to NI for OCP 97A setting; S101298988
20160621		1. Page 98 Change PWM505, PWM533 to 4.7ohm, PWM506, PWM334 to 3.3ohm, PWM372 to 1uf, PWM712 to 4.7uf, add PWM360, PWM602 at phase net, to fix NVYD power down and MOS damage issue;
20160705		PC123 change from 680pf to 82pf; S101314063
20160711		PR918 changed from 23k to 24k, op, increase for USB short to GND testing. S101296331

ITEM	DATE	CHANGE DESCRIPTION
		FOR EEP/MB
20160912		1. Page 74, change PC250, PC251, PC252 to I Page 76 change PC270 to I Page 70 change PC604 to I; S101326374
20160912		1. Page 63 change PC937 to I Page 63 change PC946 to I

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	—DC Change List—	
DATE	APPROVING AUTHORITY	REV
2014	Ant Man - Premium	A01
DATE	Wednesday, October 01, 2014	
	1	2

081716
1. Modify net name
(p.9) NXP_CK_100M_H_UTP# --> XDP_CK_100M_H_UTP_N
2. Change reference
(p.34) P160 -> P60
(p.34) J213 -> P210
(p.28) U22 -> U68
(p.28) XJ22 -> XJ68
(p.43) P150 -> P24
3. Add components for EMC request
(p.51) Reserved C1 on COM_DET#
(p.58) Reserved C2, C4, C5, C5 for audio AGND/AGND

082116
1. Delete redundant decoupling caps at CPU cavity
(p.13) DEL C256/C257/C258/C259/C260/C382
2. Modified DORA SODIMM decupling quantity based on INTEL's recommendation
(p.15) VDDQ_10uP#8 : C6, C9, C11, C12, C13, C15, C16, C86
(p.15) VDDQ_10uP#8 : C77, C78, C79, C80, C81, C82, C83, C84
(p.15) VTT_10uP1+1uP2 : C17, C20, C29
(p.15) VPP_10uP1+1uP1 : C91, C92
(p.16) VDDQ_10uP#8 : C23, C24, C25, C26, C27, C104, C105, C106
(p.16) VDDQ_10uP#8 : C35, C36, C97, C98, C99, C100, C101, C102
(p.16) VTT_10uP1+1uP2 : C108, C109, C107, C32
(p.15) VPP_10uP1+1uP1 : C109, C110

3. Modified Displayport schematic
(p.40) DEL D1, D1
4. Modified Base on NVIDIA's feedback
(p.81) Stuff MR573 and unstuff MDS

082216
1. DSW_PWRON_KB at PCI side.
(p.23) Set R144 "Not install".
(p.29) Set R161 "Not install".
2. Merge net "LPS_WAKE" & "SLP_SUS#1" to "SLP_SUS#"
(p.23) Set R144 "Not install".
(p.29) Set R161 "Not install".
3. PWRBTN_N#
(p.44) Change net name LPS_WAKE to SLP_SUS#
4. RSMRST#
(p.23) Set R142 "Not install".
5. Battery Charger EN_PU power rail
(p.40) Change R253 to "+3.3v_AUX"
6. Change resistance
(p.23) Change R648, R649 to 10k ohm.
(p.40) Change R160 to 10k ohm.
7. RSVD (C1/D1) left as "NC" based on INTEL recommendation.
(p.24) Add R1 (Not install) to GND

==== HP Review ====
9. PETS/APS header
(p.56) Change E18 to 2x7 pin header
10. USB Side/Rear Power net name
(p.41) USBV_REAR_1 -> USBV_SDE
(p.41) USBV_REAR_2 -> USBV_REAR
11. ESD Reset noise
(p.22) Add C817 near U119.
12. Series resistor on DISPA_SDI
(p.21) DEL R9390
13. L_CATER#
(p.10) Change R51 "Not install"
14. XDP naming
(p.9) Change "R4" to "E25"
16. M2_SSD naming
(p.53) Change to "J36"
17. LED for "HDD" are "HDD on"
(p.43) Add LED control at state of "HDD off" & "HDD on"
18. Change driving gates of transistors from 3.3v to 12v for I2C/AUX switching
(p.46-49)
19. Remove PO resistor due to IC with internal PD
(p.46) R373, 352, 364, 360, 362, 339

082416
1. ML_STR3
(p.30) Change R387 PD to "DGND"
2. CID_STR0/1
(p.30) Change R151 to 4.7K ohm
(p.30) Change R388 to 4.7K ohm
3. PECL
(p.29) Change R226 to "N"
4. SLP_5#/S4#/S5#
(p.29) DEL R20/R23/R24
5. PWRBTN_OUT#
(p.23) Set R648 "install"
6. PSON#
(p.29) R28 PU to +3.3V_LPS
7. PWRGD_PS
(p.29) Change R146 to 10K-Ohm and "install"
8. SKT0CC#
(p.29) Change R137 to 10M-Ohm
9. INTRUDER#
OK : (p.29) Change R488 to 10M-Ohm
10. SD_CPOD3
(p.29) Change R232 to 10K-Ohm
11. SLP_SUS#
(p.29) Change R289 to 10K-Ohm and "install"
12. SER_IRQ
(p.29) R494 "N" and PU to +3.3V_MAIN
13. BRD_ID
(p.30) Change R383 to "30.1K ohm"
14. power sequence
(p.23) Set R903 "install"
15. Memory SPD address
(p.15) XMM3 256/260 change to "0/0" -> A0 (DIMM2)
(p.16) XMM1 256/260 change to "0/1" -> A4 (DIMM1)

082516
1. Follow Realtek's suggestion to change the short pad between "GND and AGND" to 0ohm
(p.39) RS12, RS13 RS14 to 0 ohm
040616
1. (P.2)Update Block Diagram
040716
1. (P.41)Change ZF5 to 1.1A ZF6 to 2A

DB-to-SI phase

041516 (power-on issue)

1. SIO1287876 (DRAM Reset)
(p.11) Change R189 to 1K ohm and install

041916 (power-on issue)

1. SIO1287892 (Abnormal SMBUS voltage on U518)
(p.31) Change U518 to correct symbol.

051016

1. (P.43)Change the name from USB_N12_R to USB_N9_R; USB_P12_R to USB_P9_R(Observation Id: SIO1295772)

051216

1. (P.46)Add R9432, R9433, Q333 to fix DP1 DP to HDMI issue.(Observation ID SIO1294242)
2. (P.29)Change SIO SMBUS connections for NPCCD software. Add R20/R23 and connect to SM82_SCL/SM82_SDA(Observation Id: SIO1296102)

051216

1. SIO1289892 (BOM change)
- FCA timing issue
(p.37) E14 jumper change to w/o tail type
(p.56) L49 jumper change to w/o tail type
2. SIO1290563 (BOM change)
- Thermal issue
(p.13) Change to X85 : C570/C571/C572/C573/C574
3. SIO1298481 (Layout/BOM change)
- Internal PS header change to 1v6 pin due to spec change.
(p.43) Change P5 to vertical 1v6 header
4.SIO1298465 (Layout/BOM change)
- Bad Serial board assembly with right angle type connector
(p.34) Change Serial P52 to vertical type.

5.SIO1298443 (Layout/BOM change)
- Bad HDD assembly with right angle type SATA connector spec.
(p.34) Change SATA P60 to vertical type.

6. SIO1298430 (BOM change)
- Schottky diodes on DP_PWR are not meet OCP 1.1A spec.
(p.23) DEL R6422
(p.46) Change D7 to NXP_PMEG02151A (IF = 1.5A)
(p.47) Change D9 to NXP_PMEG02151A (IF = 1.5A)
(p.48) Change D3 to NXP_PMEG02151A (IF = 1.5A)

7. SIO1288253 (BOM change)
- JDP connector cannot work
(p.9) R102 change to 1.2k
8. SIO1298255 (BOM change)
- LAN_WAKE# pull-up power well
(p.39) R19 : NI

051916

1.(P177) Reserve Strip for the EQ of USB3.0 Redriver(Observation Id: SIO1297573)

052016

1.(P28) Change RNT1 (Resistors Array) to individual resistor due to there's no 2nd source for resistor array (R29,R32,R42,R43)(Observation Id: SIO1299022)

2. SIO1298069 (Layout change)
- ESD open pin installation text fail on DP ports
(p.54) Add 6.1u cap, ZC510, ZC866A, ZC8669 ZC8670
1. SIO1298182 (Layout change)
- Reserve the circuit for control Type-C QCP by SMBUS.
(p.19) Add Z96C02 Z96621 Z99460 Z99461

4. SIO1298255 (BOM change)
- LAN_WAKE# pull-up power well
(p.23) R6437 : R194#1

052416

1.(P19) TYREC should not supply power under SS. Change the power source for TYPE C from +5V_AUX to +5V_DUAL and reserve SLP_S4# footprint(ZR1-6) to control enable signal.(Observation Id: SIO1300147)

2. SIO1298430 (BOM/BRD change)
- Schottky diodes on DP_PWR are not meet OCP 1.1A spec.
P46-49)Change ZD4 to Q1: D7 to Q2: D9 to Q3: D2011 to Z02
3. (P.43) Change R976 to Ni for set HDD LED combined with BST function.(Observation Id: SIO1299363)

052716

1.(P46) Change R340,ZR345 to install(Auto EQ disable). R338 ,R339, R341, R342 to install(LED E348). Change R337 from 5.99K to 5.22K 1%.(Observation Id: SIO1299241)

053116

1.(P94/B1) Add Zr560 , NI R560 and reserve MR664 to replace PLTR512 for fix NVDDO drop issue.(Observation Id: SIO1298441)
2.(P19) Change R4244 R4255 to 53.6K for SET OCP to 0.9A(Observation Id: SIO1297575)

060116

1.(P24) Change R158 to 22K for fix iPOH1 issue(Observation Id: SIO1300324)
2.(P39) Change LAN chip to MP part WGO19LM(VER.A0_SKI2)(Observation Id: Observation Id: SIO1303177)
3.(P30) Change REV ID to SI phase.Install R386 with 16.5K (Observation Id: Observation Id: SIO1303416)

060216

3.(P43) Disable HDD LED combined with BST function.(Observation ID SIO1293306)

060616

1. SIO1296499
- Smart card KB connected to charging port can not wake up UUT from S3
(p.40) Change L63 to T1 TP5246
(p.40) R429 : Not install
(p.40) Change R205, R206 to 33k-ohm

SI-to-SIe phase

062116

1. Remove SPI ROM for dGPU(SIO1303604)
(p.89) NIMU1
2. Change Rev. ID to SiIe phase(Observation Id: SIO1309875)
(p.30) Change R387 from 10K to 1K.5k
3.Enable HDD LED combined with BST function: (Observation ID SIO1293306)
(p.43) Change R976 to I
4.Remove BBR header: (Observation Id: SIO1300703)
(p.43) Change E14 (R141-2) to Ni R275 to I
5. Change GPU PU from N16 to N17(Observation Id: SIO1309964)
(p.81-92) Change MUT PU to NVIDIA_N17M-Q3-A2

062916

2. Observation Id: SIO1313017
Change Internal USB Header(P24) to Ni for meet PCA SPEC

070416

1. Observation Id: SIO1293254
(p.17.18) Change RE-driver to new part and colay with 0 ohm resistor.

070516

1. Observation Id: SIO1314030 - Power LED blink abnormally
(p.43) Change R9429 to Ni
2. Observation Id: SIO1293254
(p.17.18) Change all EQ for RE-driver to low after confirm with AE n
N: Z98435 & Z98437 Z98441 & Z98433 Z98447 Z98449 Z98464 Z98466

070916

1. Observation Id: SIO1313223
(p.56) Change SW51 to Ni
2. Observation Id: SIO1300324: TPC401 fail
(p.24) Change R158 to 23.7K

071116

1. Observation Id: SIO1316008
(p.43) Follow HP's request to combine HDD LED with BST function.
Change below parts to I ZQ3, R976, R9426,R9425
2. Observation Id: SIO1316099
(p.17.18) Strapping resistors of USB3 re-driver IC/DQ/D05 should be 0 ohm for
PTN36001Z9943A,Z99436,Z99440,Z99442,Z99446,Z99448,Z99465,Z99467 changed to 0 ohm
3. Observation Id: SIO1316242
(p.52.53) Add 2 screw for lock M.2 module:M2NUT200, &M2NUT201.

SiIe to PV phase

072116

1. ESD fail on audio connector issue
(p.38) install U323-U326
2. Following RF's suggestion to reserve MLCC.(Observation Id: SIO1319665)
(p.51.93) Reserve ZC8671-ZC8676

1. Observation Id: SIO1316008
(p.43) Follow HP's request to combine HDD LED with BST function.
Change below parts to PROTO ZQ3, R976, R9426,R9425
2. Observation ID SIO1319435
(p.42) Change Stack USB3.0 and USB3.0-RJ45 to black one.

072716

1. Observation Id: SIO1321706 (BOM change)
- Change REV ID to PV phase. install R387 with 30.1K Ohm
(p.30) Change R387 to 30.1K Ohm.R386 with 10K.

072716

1. Observation Id: SIO1293254
(p.17/18) Remove the reserved 0 ohm resistor of USB-C redriver for better trace routing.

080816

1. Observation Id: SIO1295455
(p.51) Reserve 0805 footprint(R9438), and change P52.1, C393 connect to netM_VIN_COM

081016

1. Observation Id: SIO1318931
(p.24) Fix RTC issue:
ITAL 24M : C1602/C161 to 10pF (NPO)
ITAL 32.768K : C1640/C1640 to 12pF (NPO)

1. Observation Id: SIO1320554
(p.51) Change R9438 from 0 ohm to 24V/0.1A fuse.

081216

1. Observation Id: SIO1316008
(p.43) Follow PCA SPEC to combine HDD LED with BST function.
Change below parts to I ZQ3, R976, R9426,R9423,R339

081816

1. Observation Id: SIO1293254
(p.17/18) Change TYPE-C redriver C1/C2 to open/open since the result is pass after rework:
remove Z98437, Z98435, Z98443, Z98441, Z98449, Z98447, Z98466, Z98464

081916

1. Observation Id: Observation Id: SIO1319663
(p.38) Install TVS for fix audio ESD issue.install U323-U326

082516

1. Observation Id: SIO1331690
(P15.16)Change XMM1 XMM3 to 15u" part for meet PCA SPEC.

PV to PV2 phase

082616

1. Observation Id: SIO1332307
(P30)Change R387 to 68.8K for PV2 phase

090116

1. SIO1333089 (BOM Change)
- Power Button LED is too bright
(p.44) Change R211 to 1.2K-Ohm / R216 to 499-Ohm
(p.43) Change R339 to 10K-Ohm

2. SIO1334317 (BOM Change)
- Both entry and premium have some LEDs on board, and can be seen from the chassis vent.
(p.56) CR1 Not install

090716

1. Observation Id: SIO1293254
(p.17/18) Change TYPE-C redriver C1/C2 to high/high since the result is pass after rework:
install Z98437, Z98435, Z98443, Z98441, Z98449, Z98447, Z98466, Z98464

PV2 to EEP phase

1. Observation Id: SIO1332317
(P30)Change R387 to 10K, R386 to NI for EEP phase

090916

1. Observation Id: SIO1318331
(P24)Replace Y1 by 2ndITXC_7M24000027 for fix RTC issue.

EEP-to-MVB phase

090716

1. SIO1335375 (BOM change)
- Change "PS" wire-to-board header plating to TIN 100u" from Au 15u" per HP requirement.
(p.43) Change P5 to ACES_S0273-0000A-001 (100u" TIN)

091316

1. Observation Id: SIO1347399 (BOM change)
(P57): Due to Silkscreen Change, PCB change from REV:1.00 to REV:1.01

092016


1. SIO1333088 (BOM Change)
- Power Button LED is too bright.
(p.44) Change R211 to 1.2K-Ohm / R216 to 499-Ohm
(p.43) Change R339 to 10K-Ohm

***** 09/20 update*****
(p.44) Change R231 to 4.99K-Ohm / R216 to 100-Ohm
(p.43) Change R339 to 1.8K-Ohm

2. SIO1348966
- Change Thermal header plating from Au 15u" to TIN 100u".
(p.31) Change P162 to L85,111T220808-0B11


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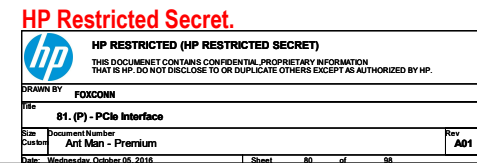
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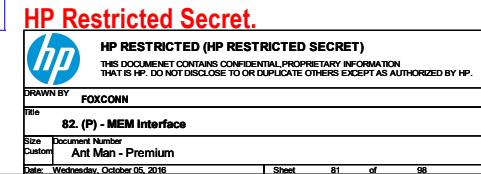
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3V3 AON



FRAME BUFFER B GPU INTERFACE

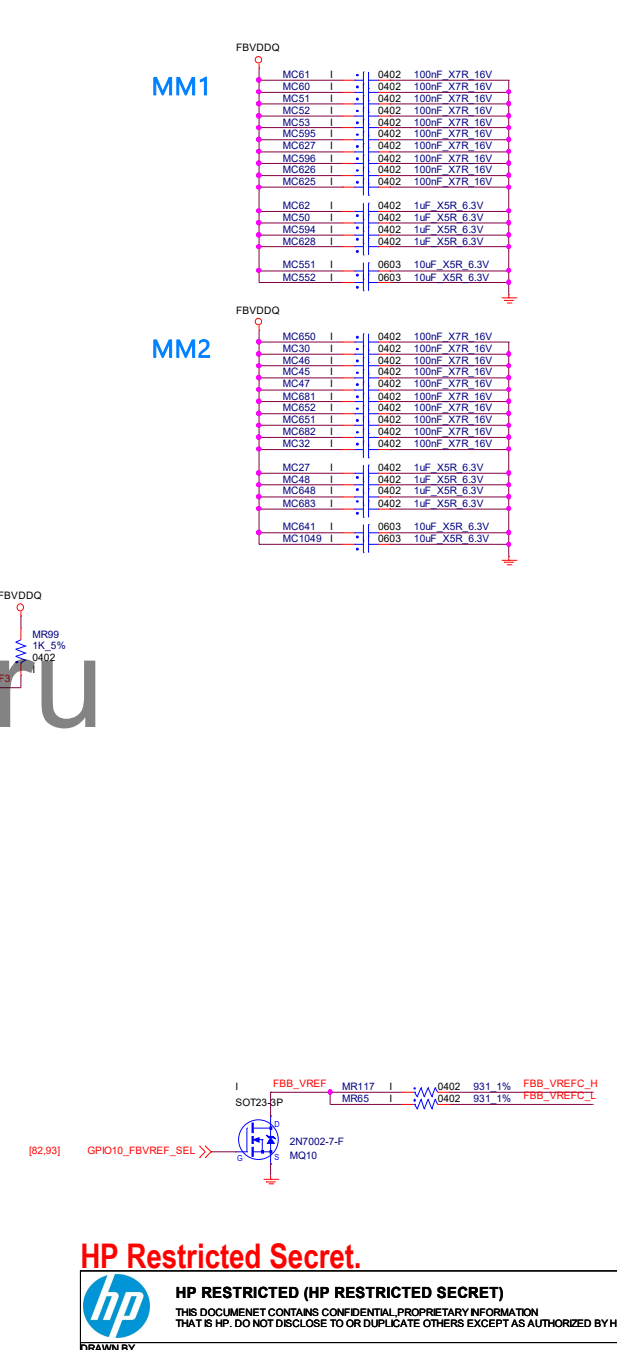
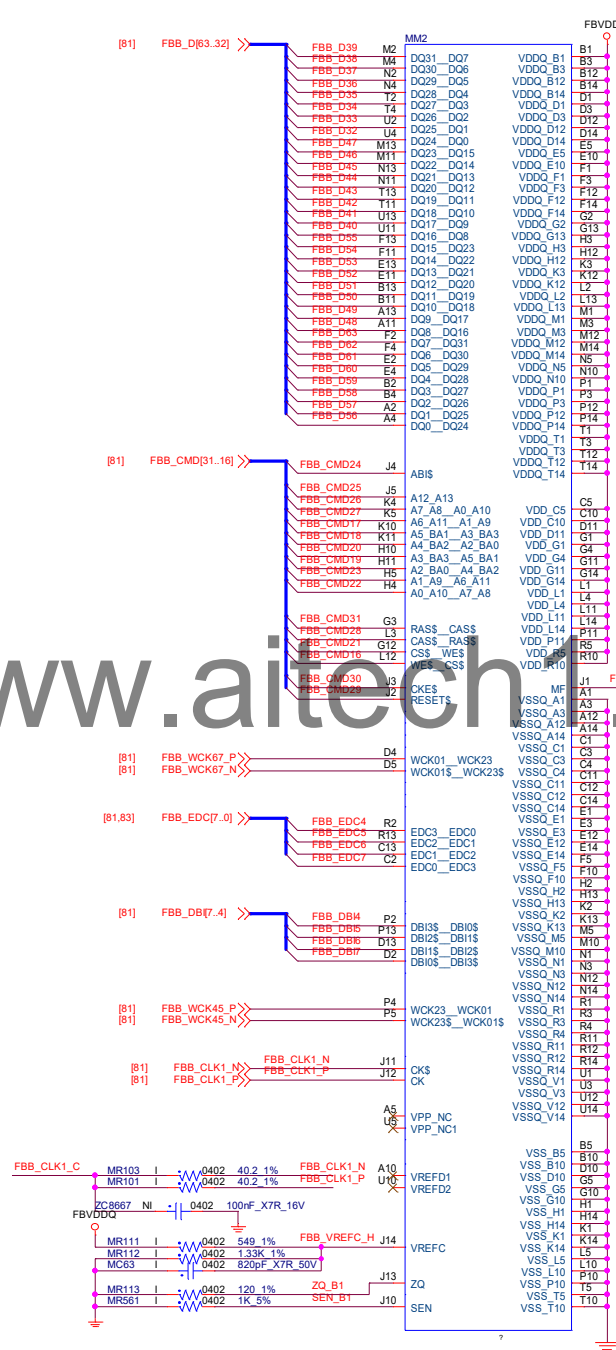


FRAME BUFFER PARTITION A [63..32]



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83. (P) - GDDR5 A							
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FRAME BUFFER PARTITION B [63..32]



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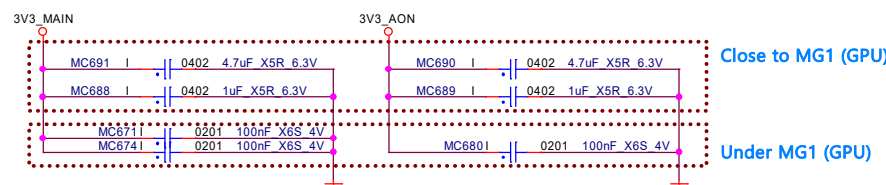
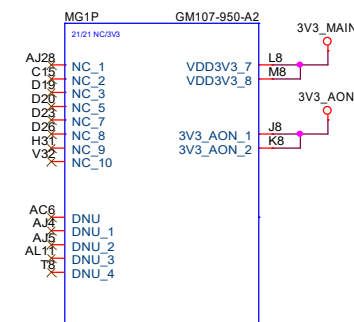
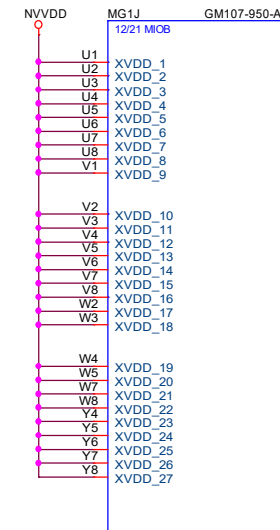
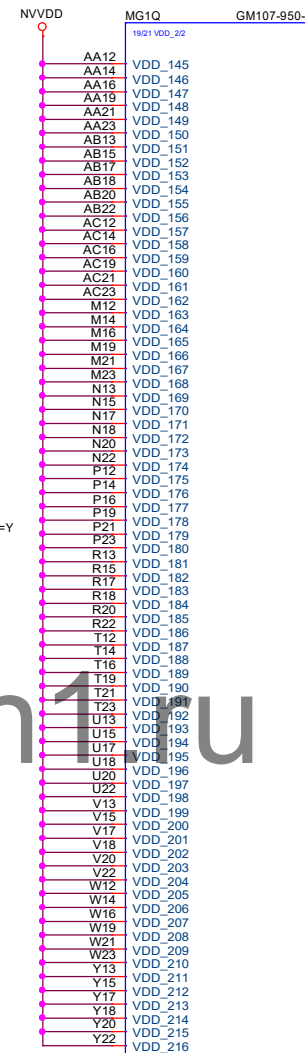
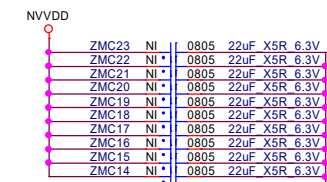
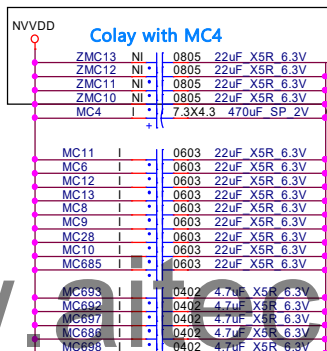
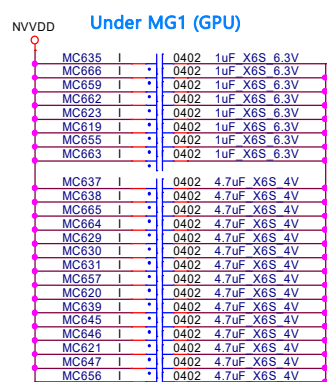
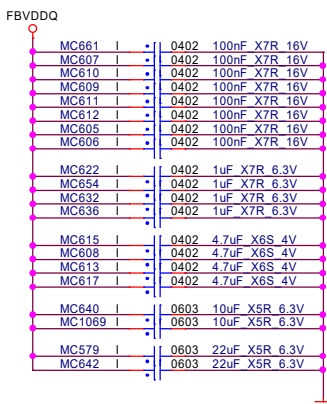
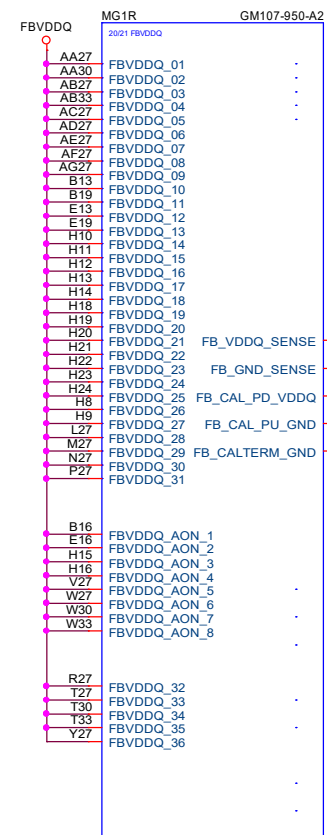
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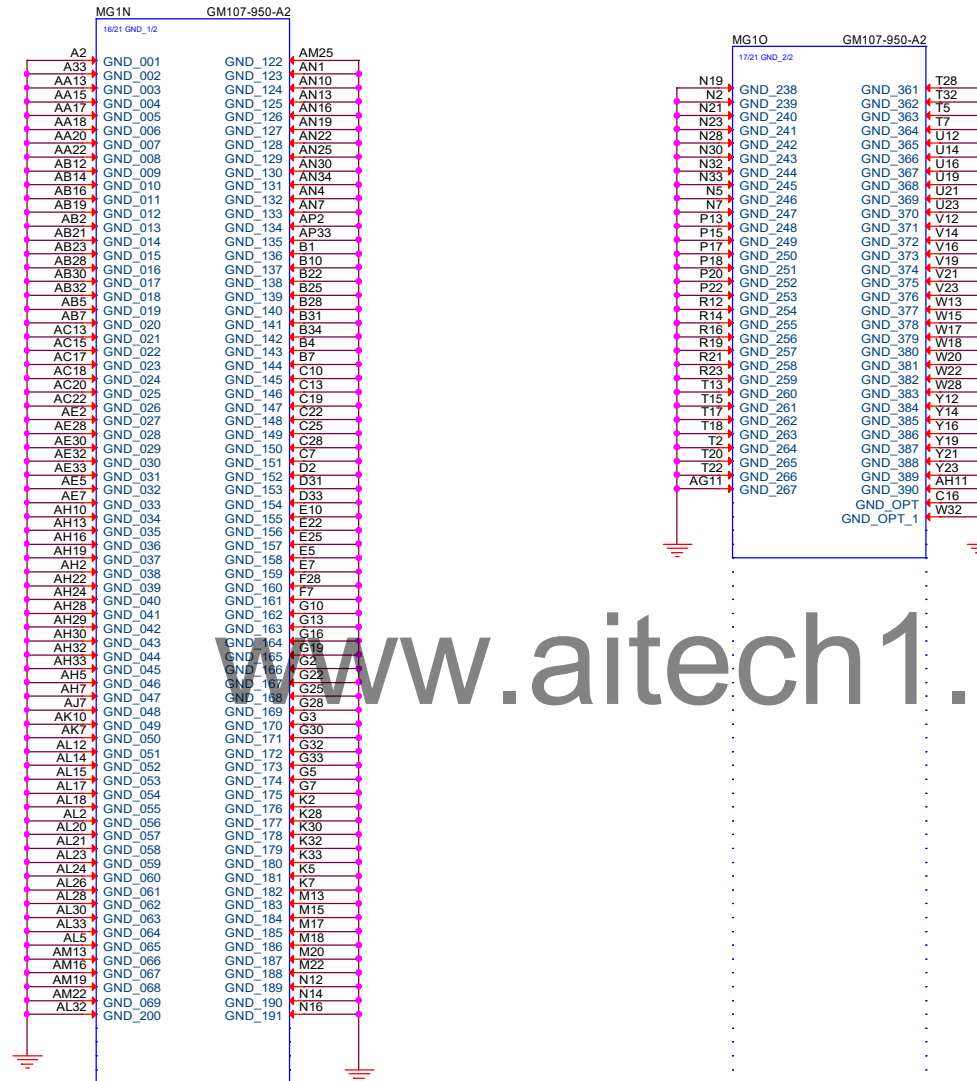
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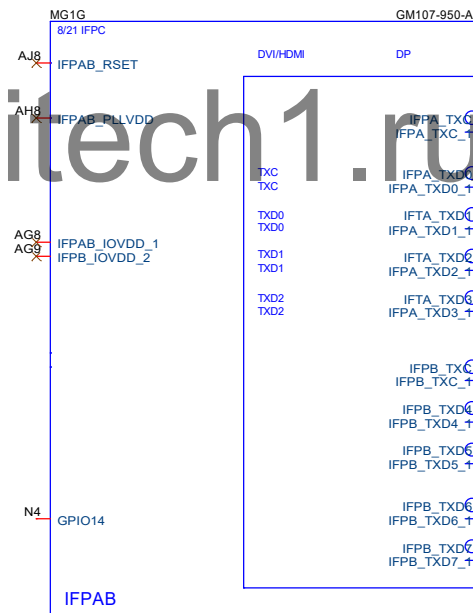
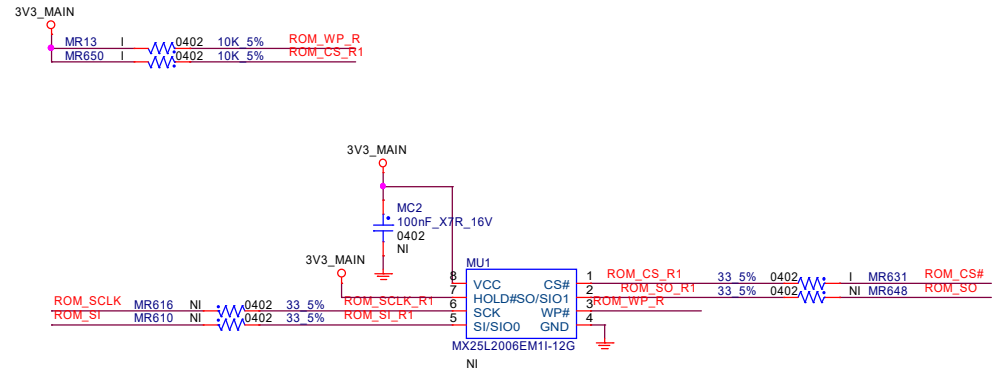
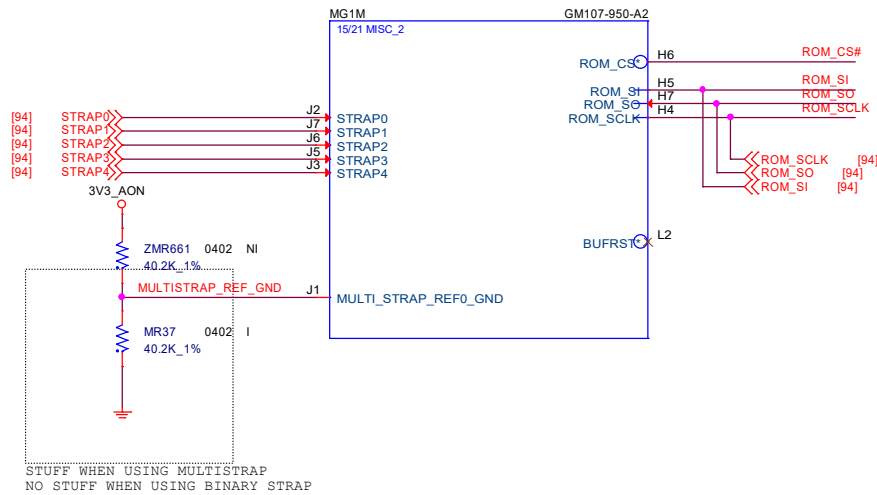
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LVDS, VBIOS



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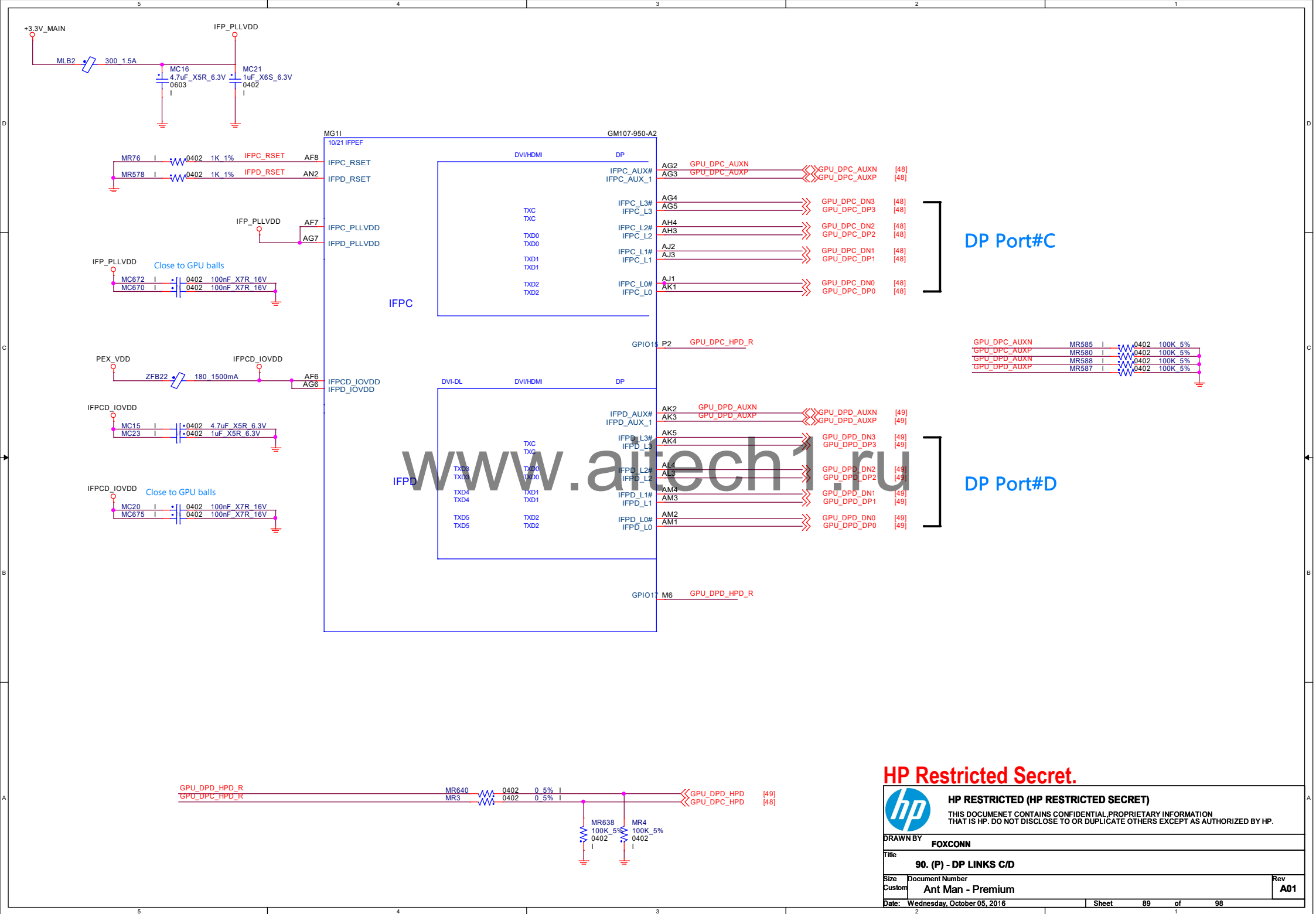
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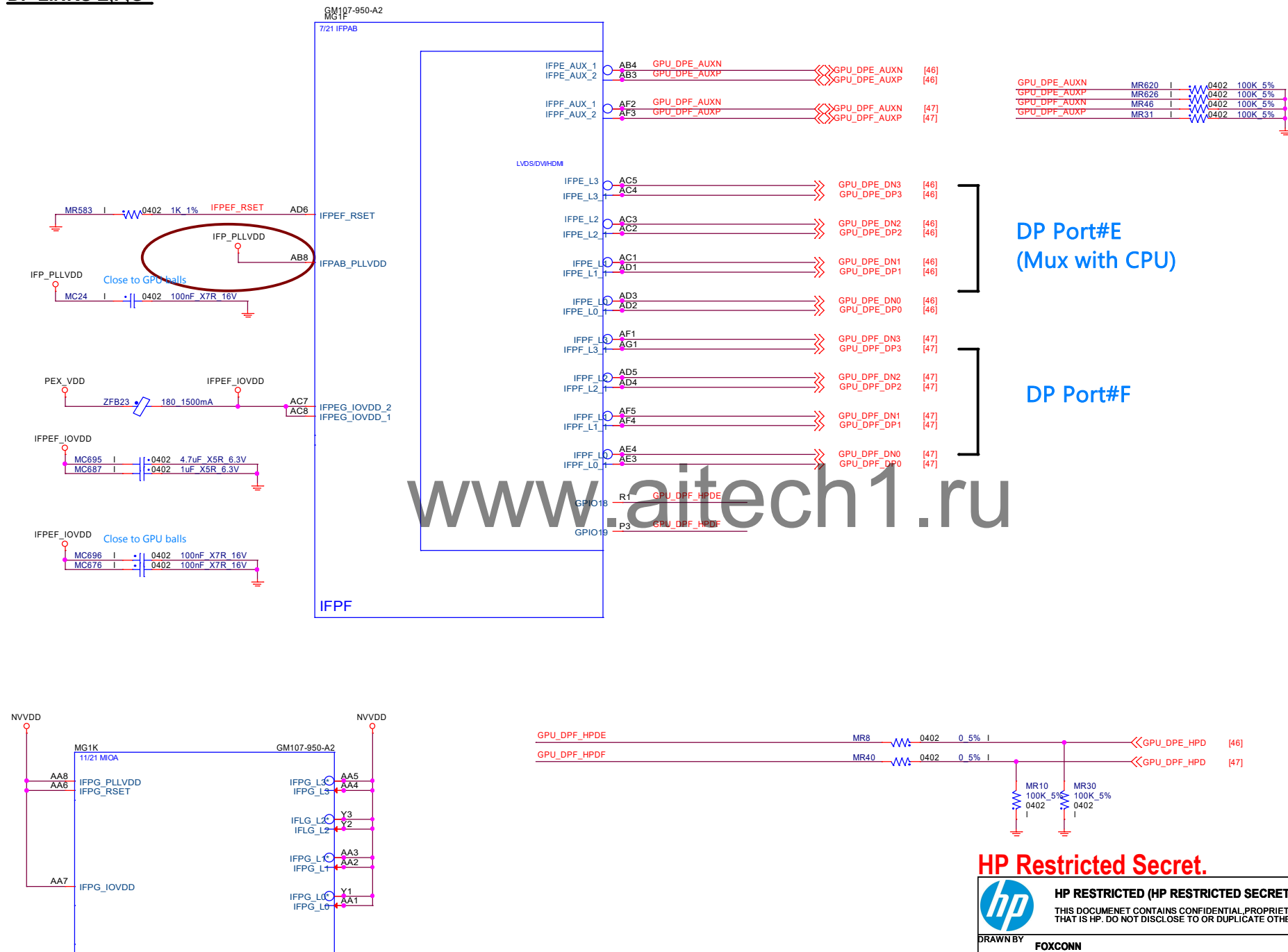
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DP LINKS E.F.G



DP Port#E
(Mux with CPU)

DP Port#F

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92. (P) - DACA PLL/XTAL

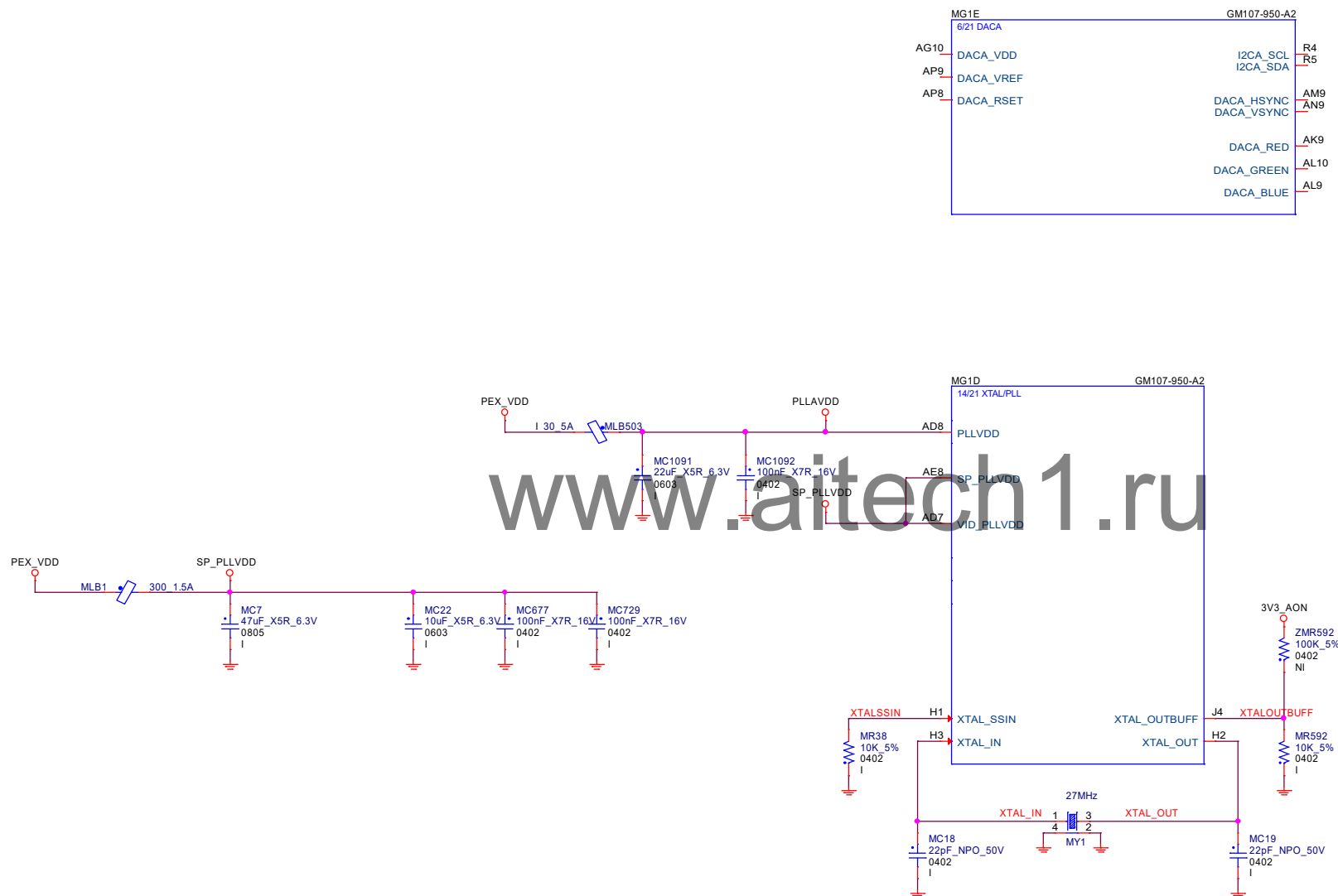
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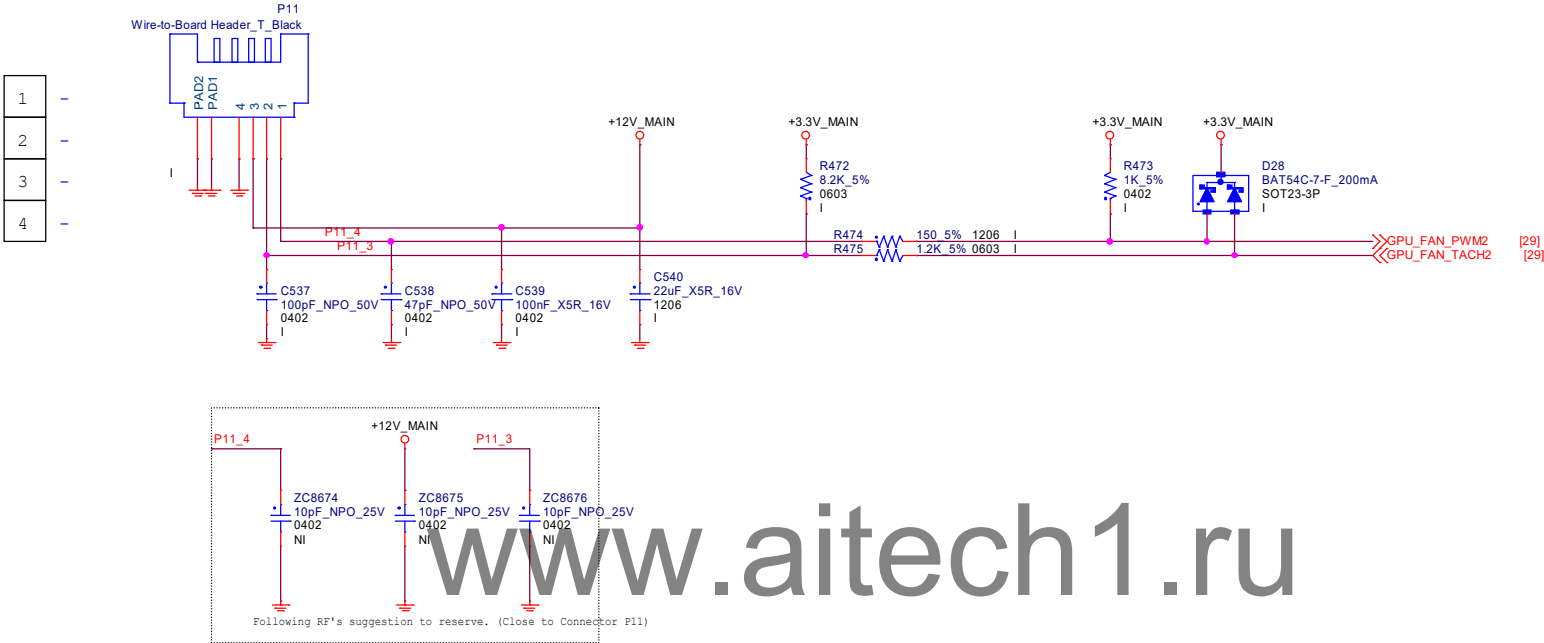
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MXM FAN



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GPIO,JTAG,TEMP SENSOR



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94. (P) - GPIO

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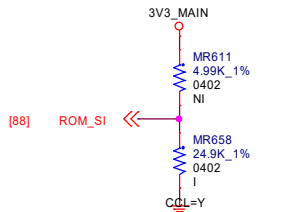
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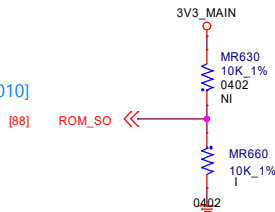
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RAM_CFG_STRAP



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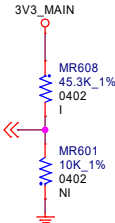
DEVID_SEL / PCIE_CFG / SMB_ALT_ADDR / VGA_DEVICE_STRAP



[3/2/1/0] = [0000]

SORx_Exposed_STRAP

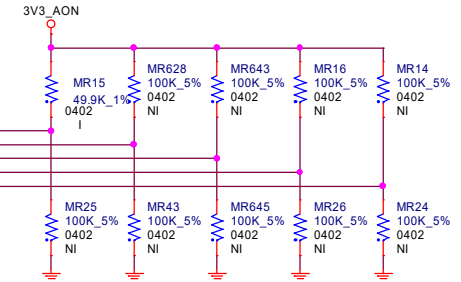
Define audio capability on each digital display.



[88] ROM_SCLK

[3/2/1/0] = [1110]

[88] STRAP0
[88] STRAP1
[88] STRAP2
[88] STRAP3
[88] STRAP4



GB4B-128 Straps

Maxwell Bit Signal Values

ROM_SI	03: RAMCFG[3]				
	02: RAMCFG[2]				
	01: RAMCFG[1]	0111	128Mx32 128bit Samsung	Primary	
	00: RAMCFG[0]	0101	128Mx32 128bit Elpida	Third	
ROM_SO	03: DEVID_SEL	0	DEFAULT		
	02: PCIE_CFG	0	HS	1	LS
	01: SMB_ALT_ADDR	0	DISABLED	1	ENABLED
	00: VGA_DEVICE	0	DISABLED	1	ENABLED
ROM_SCLK	03: SOR3_EXPOSED	0	DISABLED	1	ENABLED
	02: SOR2_EXPOSED	0	DISABLED	1	ENABLED
	01: SOR1_EXPOSED	0	DISABLED	1	ENABLED
	00: SOR0_EXPOSED	0	DISABLED	1	ENABLED
STRAP0	100kOHM PULL UP TO 3V3_AON				
	RESERVED				
STRAP1					

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Multilevel Straps

0000	4.99K to GND	1000	4.99K to VCC
0001	10K to GND	1001	10K to VCC
0010	15K to GND	1010	15K to VCC
0011	20K to GND	1011	20K to VCC
0100	24.9K to GND	1100	24.9K to VCC
0101	30.1K to GND	1101	30.1K to VCC
0110	34.8K to GND	1110	34.8K to VCC
0111	45.3K to GND	1111	45.3K to VCC

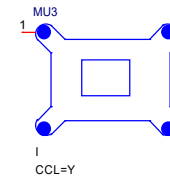
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X6
NO STUFF

MEC1
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X6
NO STUFF

MEC1
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X6
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X6
NO STUFF

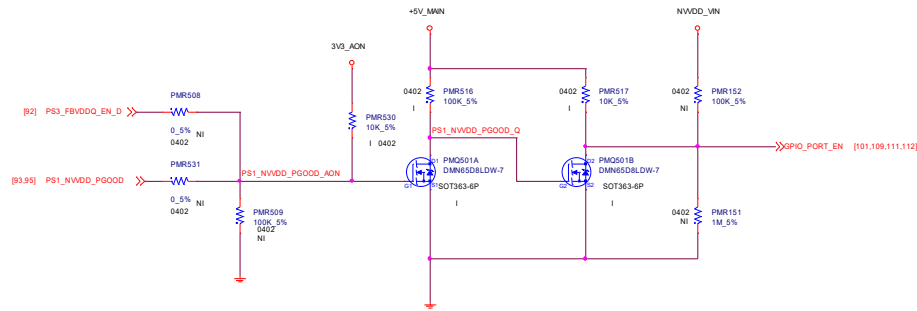
Screw hole for GFX bracket



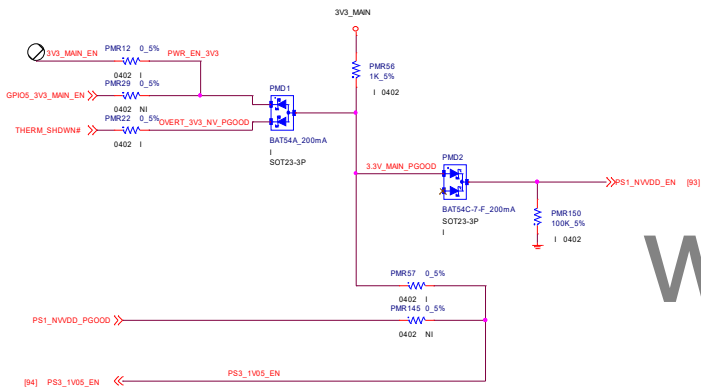
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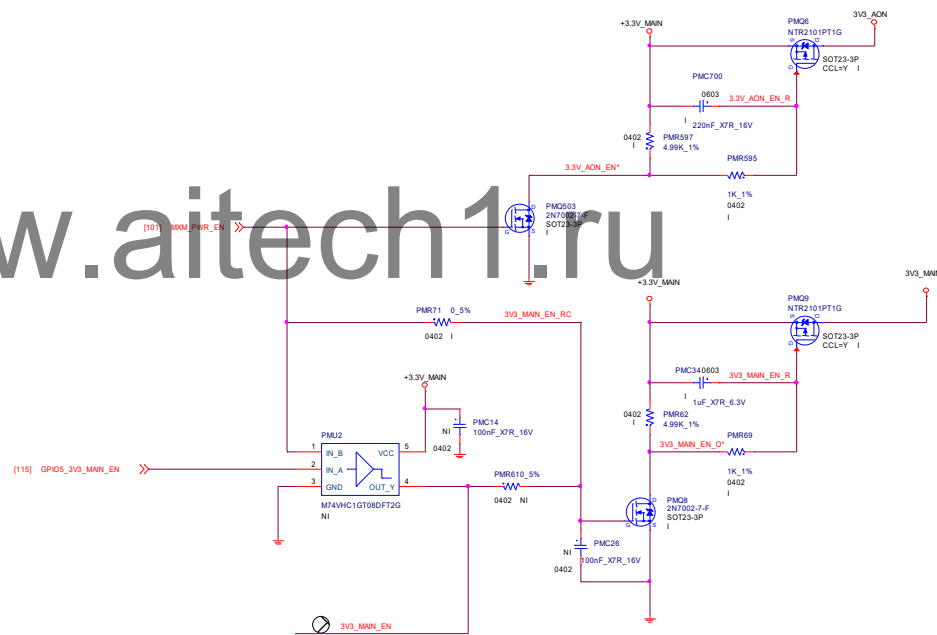
GPIO PROTECT ENABLE



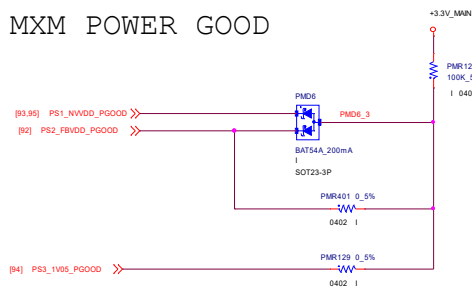
NVDD&PEXVDD ENABLA



3V3_MAIN&3V3_AON ENABLE



MXM POWER GOOD



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